Gillman, AR (Tony)

From: Gillman, AR (Tony)
Sent: 20 December 2002 14:15
To: Gillman, AR (Tony)
Subject: Notes of Phone Conference - 06/12/2002

Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference - 6th December 2002

Heidelberg: **Paul Hanke, Karsten Penno**
Birmingham: **Richard Staley**
Mainz: **Uli Schaefer**
QMUL: **Eric Eisenhandler**
RAL: **Norman Gee, Tony Gillman, Viraj Perera**
Stockholm: **Christian Bohm, Attila Hidvegi, Sam Silverstein**

1. Birmingham

Richard (with notes from Gilles) summarised the status of the CPM testing:

- LVDS de-serialised parallel output data can now be captured correctly in the Serialisers
- Serialisers -> CP chips pcb routing is all OK, but errors seen in some of the data captured in CP chips
- Biggest problem is difficulty in achieving timing calibration on all 108 channels into CP chips - firmware design still under investigation
- HIT outputs from CP chips are seen correctly
- Serialiser DAQ data from ROC -> G-link inputs are seen correctly
- DAQ G-link data -> DSS tests will be done very soon
- Backplane 160 Mbit/s data show significant reflections and attenuation - impedance of some tracks ~39 ohm cf 56 ohm design figure

2. Heidelberg

a) Karsten summarised the good progress on ASIC/MCM tests:

- Data can now be read out via the real-time data path via VME - all the necessary firmware is working
- With no inputs to the ADCs, noise data are latched into memory and recorded, with occasional BCID outputs seen
- The next step is to provide known analogue inputs from the video DAC system
- The serial interface to the ASIC needs more work in order to configure the ASIC into a known state (it should currently be in the default state)

b) Paul summarised the progress on accelerating the PPM schedule:

- The Xilinx XCV50E will be checked very soon for its suitability as an LVDS fan-out device, using long cable links with pre-compensation and a realistic connector scheme - BER measurements will also be made
- LVDS fan-out daughter-card layout will be started at the end of January 2003
- The DAQ architecture will change to the CP/JEP one, feeding raw uncompressed data from each PPM via G-links
- RAL will design the small rear G-link daughter-card, with specifications from Heidelberg and RAL. PPM -> ROD cable routing (rear-PPM -> ROD-front-panel) needs to be worked out to minimise lengths
- The ReM-FPGA (XCV1000E) firmware is the biggest problem - lack of people to write it, although code is now simpler without compression
- The PPM specifications will be updated ASAP to reflect these changes
- With all these changes, the first PPM (with 2-3 MCMs) could be available by mid-2003 - a new schedule is being prepared
- A further batch of G-link Tx (and Rx) chips needs to be ordered ASAP - number estimated to be ~200

3. Mainz

Uli reported on the JEM status:

a) Firmware and tests:

- Andrea has fully coded the sum merger real-time data path
- The crate merger code has been fully simulated, and the Et system merger code has also been simulated
- The Etmiss system merger code will be simulated as soon as the software for the generation of LUT contents is available

- The new input synchronisation code on the input FPGAs has been tested, and the automatic detection of the optimum sampling phase seems to work
- The phase detection scheme requires alternating data (0,1,0,1,...) on the lsb of the LVDS data word, so should be compatible to the CP synchronisation scheme. The additional delay of 0 or 1 tick will be under software control. A different synchronisation pattern (00000001 on the lsb) will be required from the PPr playback memory

b) Hardware:

- The new EP89 cable driver for the G-link outputs has arrived and will be mounted on JEM0.1
- Bruno is working on the JEM1 Input daughter-card, consisting of 1 FPGA XCV1500 and 4 6-channel de-serialisers. The daughter-card concept minimises the lengths of the LVDS tracks and the FIO links. Only for the 480 Mbit/s traces will be in microstrip form
- There are minor updates to the JEM1 documentation at: http://www.uni-mainz.de/~uschaefe/browsable/JEMdocs/JEM1/
- Specification updates for a JEM1 mini-review to be held on 11-12 December will be made available at: http://www.uni-mainz.de/~uschaefe/browsable/JEMdocs/JEM1/

4. RAL

Viraj reported on the hardware and firmware status:

- Two TTCdec cards designed for the new TTCrx chips have been assembled and are ready for testing
- Loading of the CMM FPGA configuration flash memory from VME is still being worked on
- It is intended that all CMM design updates are completed by the end of December

5. Stockholm

Sam reported on the Jet code status:

- A random data sample of 3M test vectors have exercised the jet algorithm correctly in simulation
- Andrea has supplied the remaining energy algorithm firmware to merge with the jet algorithm code
- Attila is working on achieving full-speed operation of the combined code, but currently has problems with the synthesis tools, relating to the 40MHz/80MHz clocks
- Backplane characteristic impedance and propagation delay measurements will be made before the end of December

Next Phone Conference - 20th December 2002 at 10:00 GMT

Tony Gillman