CPM test plans

Low level H/W testing

TTCdec	JTAG Tester	Crate	TCM	VMM	CPU	PC	DSS	CMM Slot Adapter	Slow LVDS DB	Fast LVDS DB	CPM	ROD
1		1										

- Check incoming voltages
- Internal supply plane
- DC/DC within specs.
- Current consumption...

Boundary Scan - CPLD/FPGA configuration

- Three JTAG ports:
  - ROC, VME controller,I2C, hit and TTCrx
  - Twenty serialisers
  - Eight CP chips VME interface checke
- Scan between VME controller and previous blocks

TTCdec	JTAG Tester	Crate	TCM	VMM	CPU	PC	DSS	CMM Slot Adapter	Slow LVDS DB	Fast LVDS DB	CPM	ROD
1	1	1										

Clock

- Onboard clock oscillators are running
- Check distribution and quality of 40 MhZ with testpoints

TTCdec	JTAG Tester	Crate	TCM	VMM	CPU	PC	DSS	CMM Slot Adapter	Slow LVDS DB	Fast LVDS DB	CPM	ROD
1		1	1									

Basic VME access

- VME controller: R/W mother ID,…
- TTCrx access
- DCS

TTCdec	JTAG Tester	Crate	TCM	VMM	CPU	PC	DSS	CMM Slot Adapter	Slow LVDS DB	Fast LVDS DB	CPM	ROD
1		1	1	1	1	1						

CP chip test - part I

- Play back memory (TTC controlled) + Scan Path F/W:
  - Timing: test vectors used for GTM test, 128 events stored in DP RAM
  - Connectivity: simple pattern in DPRAM (0000 0001 ...) track down to each pin input
  - test vectors used for GTM test
- BC-mux scheme
- “Pseudo” Real Time Data from DP RAM tested with CMM emulator mounted on backplane (1 slot tested) - Hit block algorithm tested.
- More? Need dedicated card re-routing signals from CP chips via backplane to CP chip under test: CP algorithm tested.

TTCdec	JTAG Tester	Crate	TCM	VMM	CPU	PC	DSS	CMM Slot Adapter	Slow LVDS DB	Fast LVDS DB	CPM	ROD
1		2	1	1	2	1	1	1	1			

Serialiser Algorithm

- BC-mux: data loaded in DSS RAM and read back in the serialiser DP RAM

TTCdec	JTAG Tester	Crate	TCM	VMM	CPU	PC	DSS	CMM Slot Adapter	Slow LVDS DB	Fast LVDS DB	CPM	ROD
1		2	1	1	2	1	5			10		

CP Algorithm - Part II

- Supplementary CPMs provide data to fully test CP algorithm via their playback memory or …
- …by sharing DSS Source modules

TTCdec	JTAG Tester	Crate	TCM	VMM	CPU	PC	DSS	CMM Slot Adapter	Slow LVDS DB	Fast LVDS DB	CPM	ROD
1		2	1	1	2	1	5			10	2	

LVL1 Signal - Real Time Data

With the addition of a ROD, L1 path is tested:

- ROC DAQ
- ROC RoI
- BER measurement of Real Time and L1 path.s

TTCdec	JTAG Tester	Crate	TCM	VMM	CPU	PC	DSS	CMM Slot Adapter	Slow LVDS DB	Fast LVDS DB	CPM	ROD
1		3	1	1	3	1	6	1	1	10	2	1