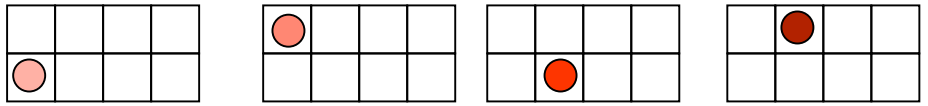
CPM Status

Firmware Status

- ROC DAQ / RoI
  - Generated L1A signal, to test data on Glink port, via modification in Richard's TTCrx controller
  - Transfer data successfully between DPR and Fifo of Srl/CP/ROC , and as a function of required Nslice
  - Data available on Glink output but we need to know if they are OK (Logic Analyzer/ROD?)
- Hit: not tested yet as focus went on real time data path between SRL and CP chip

CP chip: algorithm test

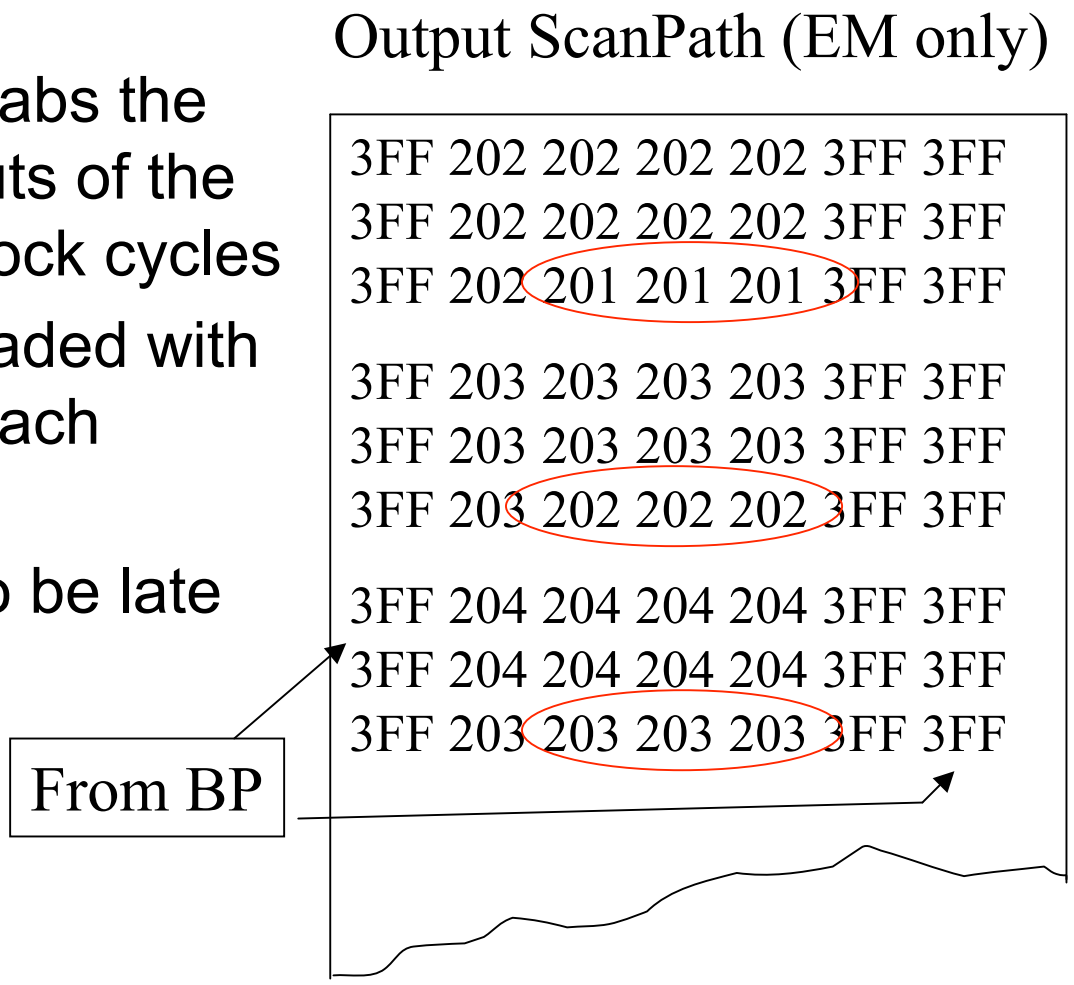
- Algorithm works for very basic kind of non-physics data



  - All isolation threshold high (0x3F), cluster thresholds vary from 0x0 to 0xF
  - Cp chip returns RoI at the right place with the right passed threshold value (double checked with VHDL model)
- But some RoIs were not output: after investigation, input data were not the one expected…

CP chip: back to "ScanPath" mode

- ScanPath register grabs the value of the 108 inputs of the CP chip during 26 clock cycles
- DPR of SRL were loaded with a ramp of value on each trigger tower cells
- Some data appear to be late by one clock tick



CP chip: Delay and Clock

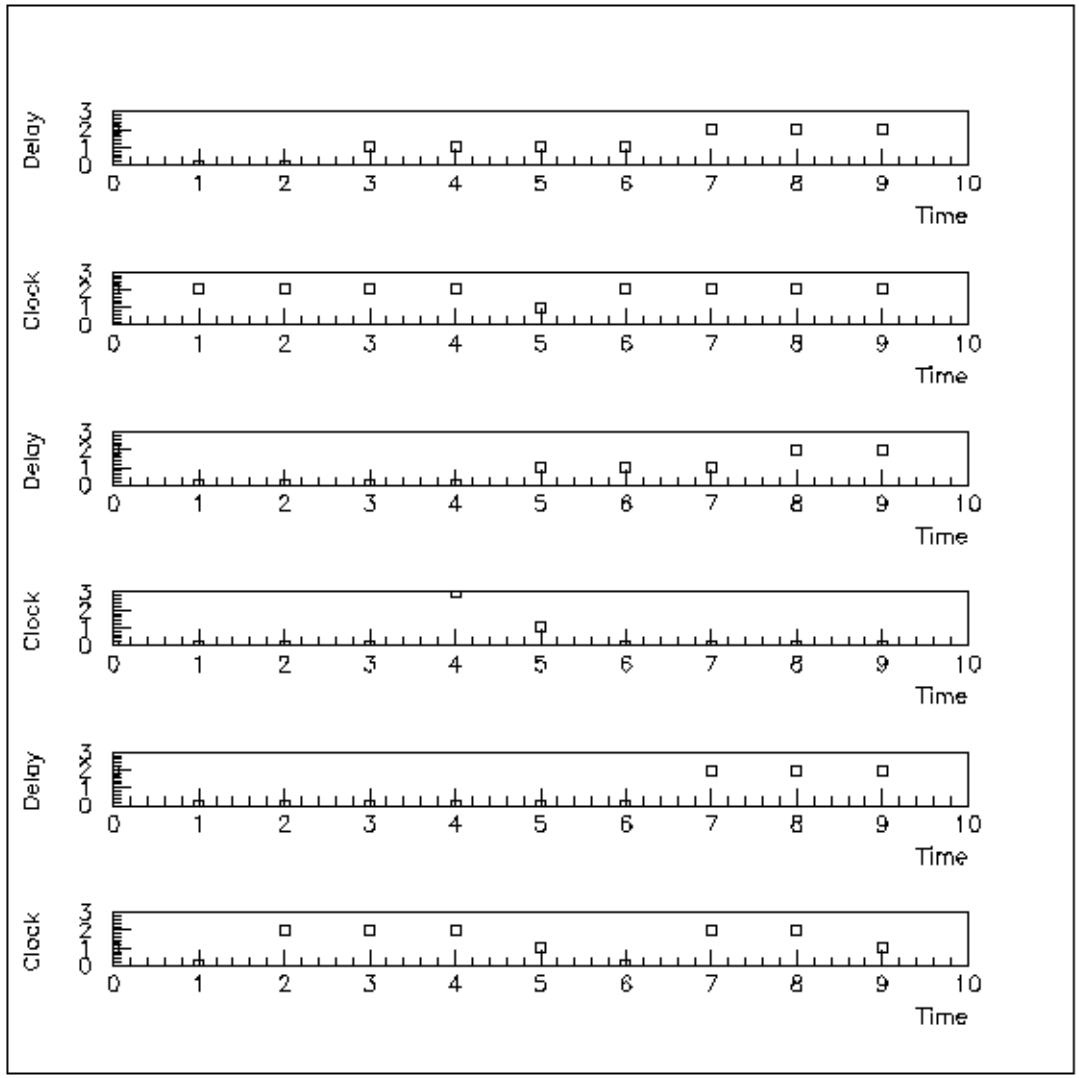
- Late data have a delay always set to 3, I.e 3x6.25 ns, other delays are set to 0
- We understand that this data are late by a couple of 100 ps , just on the edge of the clock, and missed the next tick
- The calibration process of the CP chip check that the calibration pattern is recovered correctly after deserialisation, but not correctly timed between channels
- Ian delivers a new F/W version where serialised data are generated halfway during one clock cycle, therefore requiring to the CP chip to add a delay of 2x6.25ns to recover them correctly, and avoiding to work on the edge of the clock
- New SRL F/W delivered data on time…but now , some data appear to be corrupted

Investigation of calibration process

- Previous test were done with a home-made 40 MHz clock delivered to CP and SRL chip
- Test are now performed with a TTCdec card, and two independent deskewed 40 MHz clocks are delivered to the CP and SRL chips
- As no I2C access is available, the delay between the Deskew1 (Srl) and Deskew2 (CP) clock is handled via TTC command (B channel)
- The available step is of 104 ps

Clock and Delay: early investigation

- Each step of delay is of 1.57 ns
- Even if calibration process is ok for all channels, some data appear wrong from time to time
- Need plot Error%Delay (to come soon…)



Corrupted data investigation

- Data pattern:

  0011 0100 0101 …expected
  0011 1100 0101 …seen

- Xtalk suspected…but after fired all surrounding channels, data values are not affected
- I can find a set of delay for deskew1 and deskew2 where everything is working correctly for all channels…but the range is very narrow, order of 1.5 ns

Solutions?

- Change calibration process with a different pattern? Different delays?
- Put ChipScope in ScanPath F/W
- Need a S/W calibration process for CP chips?
- CP F/W will need to be changed to enable reset of DLLs:
  - by changing Clock spec., DLLs end up losing their lock: DLLS locks again after re-loading the F/W configuration
  - Clock will have some holes during LHC operation
  - Applied also to SRL

Parallel work - Checklist

	Yes	No
LVDS testing required:		
– 5 DSS source	1	4
– 10 LVDS daughter card	3	8
– 20 LVDS cables	2	18
Backplane neighbourhood CPM testing:		
– 1 Loop I/O card (extender)	1	
Backplane CMM		
– 1 DSS Sink		1
– 1 GIO card	1	
– 1 CMM emulator	1	