8th Workshop on Electronics for LHC Experiments – Colmar 2002

Quick browse…

http://lhc-electronics-workshop.web.cern.ch/LHC-electronics-workshop/2002/CALMUON.htm

Plenary session – part I

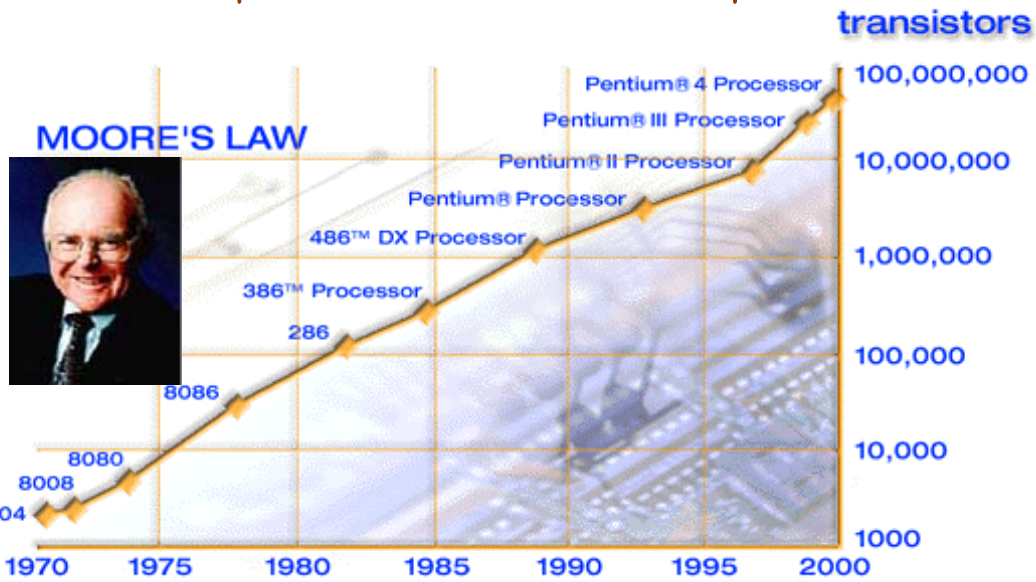
- **LHC Physics Goals explained for Engineers**
  P. Sphicas (CERN)
- **LHC Beam Instrumentation Detectors and Acquisition Systems**
  R. Jones (CERN)
- **Trends in microelectrics and nanoelectronics and their impact on HEP instrumentation**
  P. Jarron (CERN)
- **Managing for Quality in the Electronics Industry**
  S. Kelly (Motorola) P14
- **LHC DAQ Systems**
  S. Cittolin (CERN).
- **First-level trigger systems at LHC N. Ellis (CERN)**
- **Summary of the JCOP Workshop III**
  W. Salter (CERN)
- **Radiation Assurance of LHC electronics**
  P. Farthouat (CERN)

Plenary Session - Part II

- **Grounding and Shielding Techniques for Large Scale Experiments**
  M. Johnson (Fermilab)
- **LHC Machine and Experiment Interface Issues**
  E. Tsesmelis (CERN)
- **Trends in high speed, low power Analog to Digital converters**
  L. Dugoujon (STMicroelectronics, Grenoble) .
- **Distributed Processors allow revolutionary Hardware / Software partitioning**
  J-L. Brelet (Xilinx Inc, Sophia Antipolis)
- **Technology Transfer**
  R. Amendolia (CERN) .
- **Timing Distribution at the LHC**

Scaling and Moore's Law

Trends in microprocessor development



4004 in 1971

Pentium4 in 2000

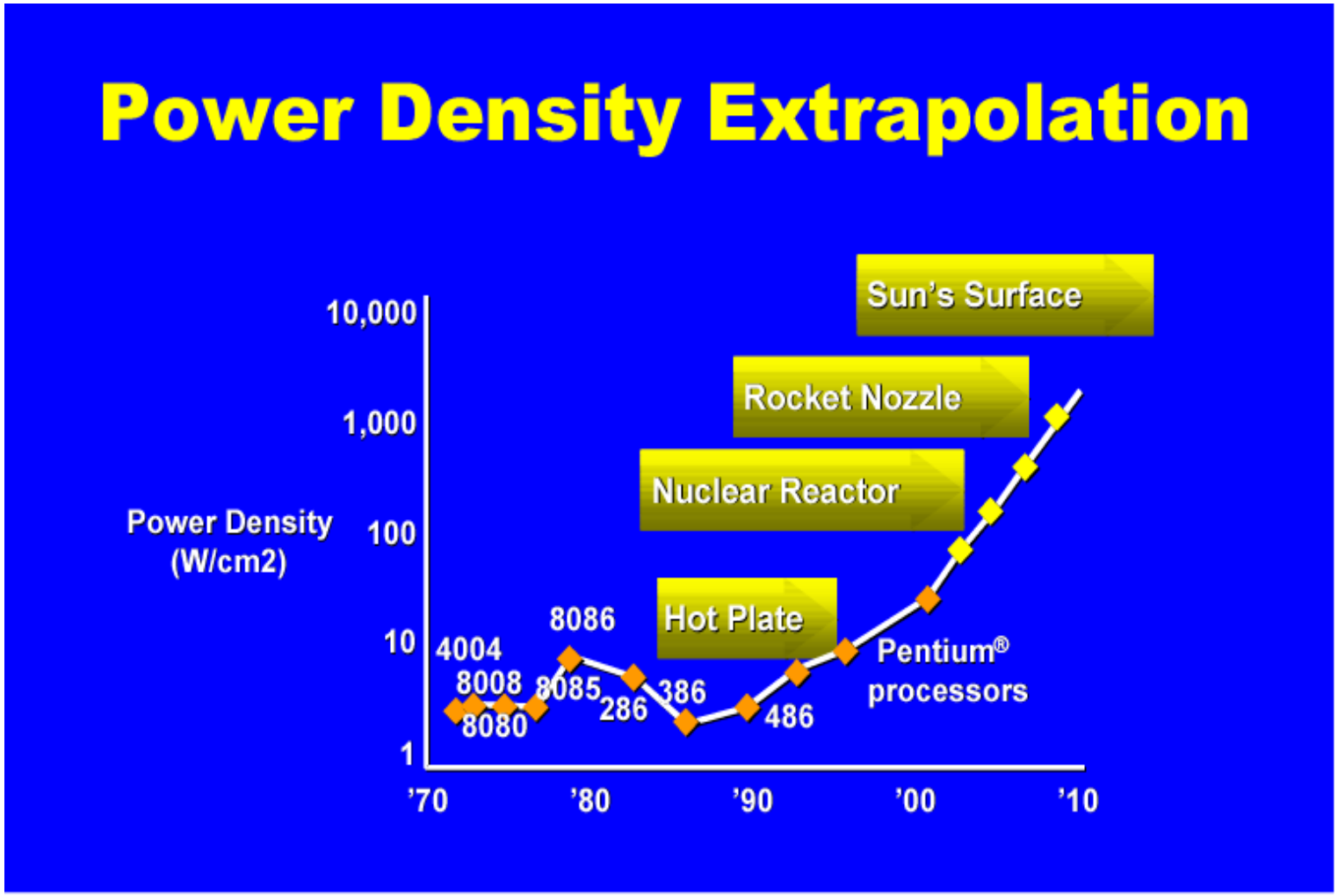
Si starting block

4004	1971	2,250
8008	1972	2,500
8080	1974	5,000
8086	1978	29,000
286	1982	120,000
386™ processor	1985	275,000
486™ DX processor	1989	1,180,000
Pentium® processor	1993	3,100,000
Pentium II processor	1997	7,500,000
Pentium III processor	1999	24,000,000
Pentium 4 processor	2000	42,000,000

Source: Intel

Power density trends and limits

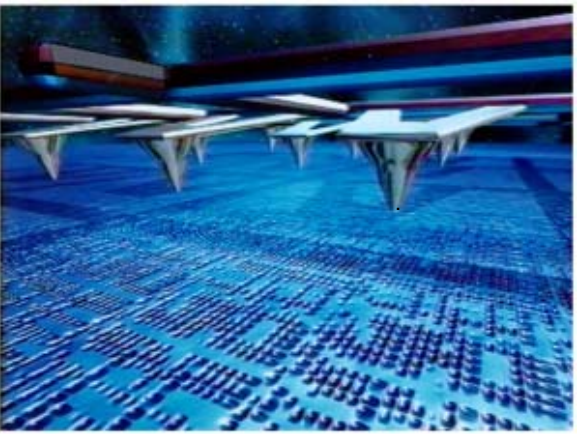
Thermodynamic ultimately limits progress of microelectronics

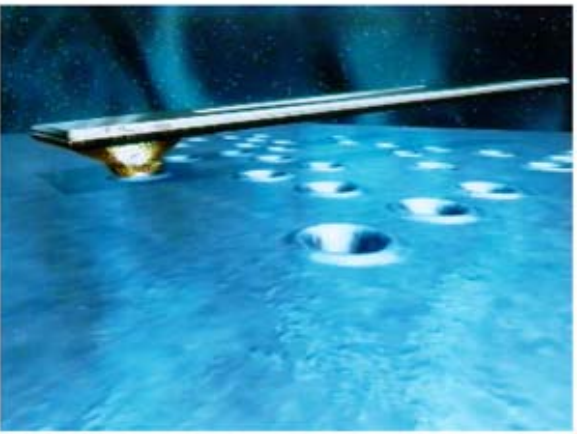


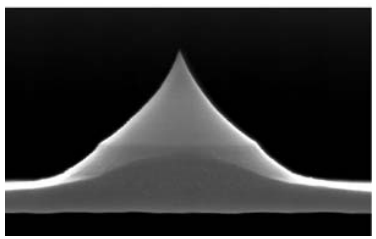
Pat Gelsinger's slide from ISSCC2001 - Intel

Nanotechnology could surprise us!

A good old memory concept revisited: nano-mechanical memory

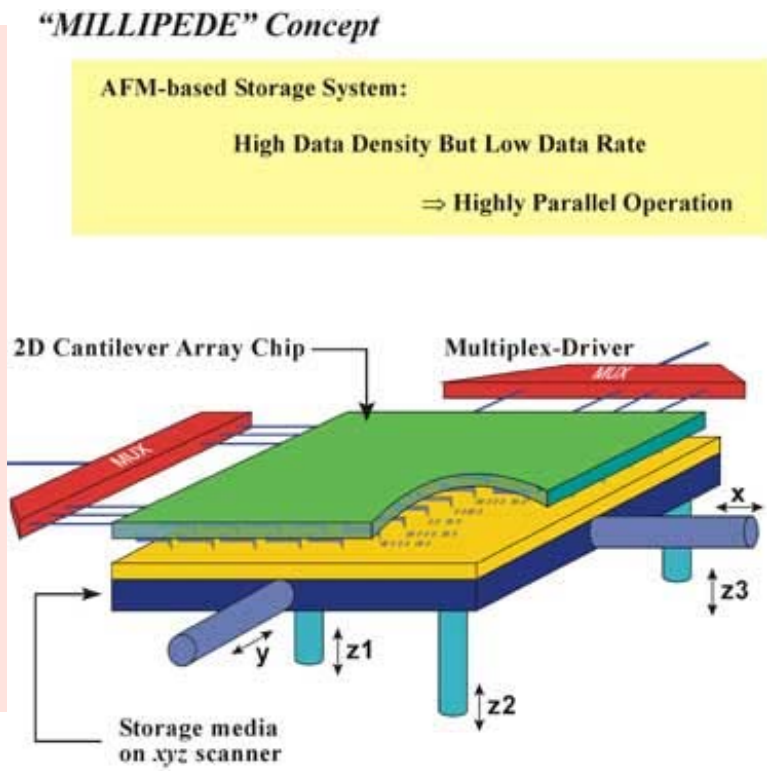






This technique is capable of achieving data densities in the hundreds of Gb/in² range, well beyond the expected limits for magnetic recording (60–70 Gb/in²).

June 11, 2002 Zurich Using an innovative nanotechnology, IBM Zurich has demonstrated a data storage density of one trillion bits per square inch — 20 times higher than the densest magnetic storage available today.



http://www.research.ibm.com/resources/news/20020611_millipede.shtml

Optimal Solutions Enabled by On-Demand Architectural Synthesis

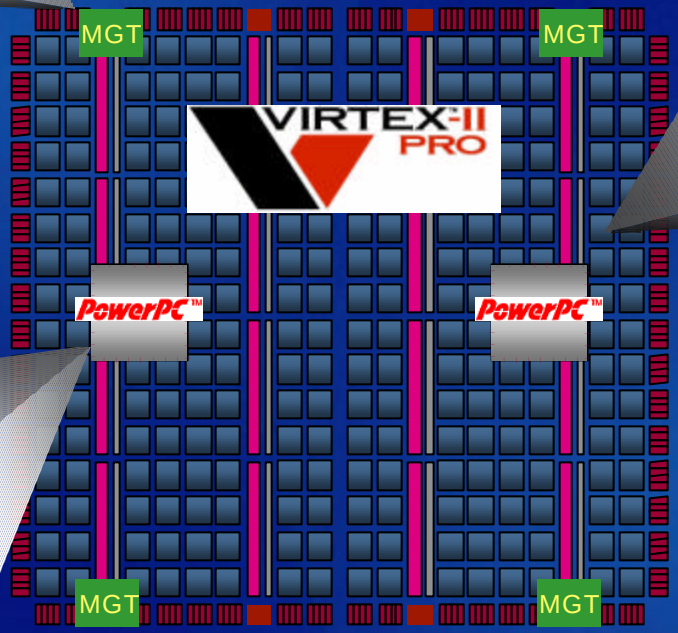
- **Hardware:**
  - Physical Layer
  - Memory Interfaces
  - Protocol Bridges
  - FSM
  - Signal Processing
  - Encryption
- **Software:**
  - Protocol Stack
  - User Interface
  - Diagnostics
  - Control
  - Signal Processing
  - Encryption

Virtex-II Pro Platform FPGA

RocketIO

- 3.125 Gbps Multi-Gigabit Transceivers (MGTs)
- Supports 10 Gbps standards

  Up to 24 per device



VIRTEX-II Fabric

- IP-Immersion™ Fabric
- ActiveInterconnect™
- 18Kb Dual-Port RAM
- Xtreme™ Multipliers
- 16 Global Clock Domains

PowerPC™

- PowerPC 405 Core
- 300+ MHz / 450+ DMIPS Performance
- Up to 4 per device

XILINX

Conclusion

- Distributed Processors Allow Flexible HW / SW Partitioning:
  - Optimal mapping at the module level
  - Offer to design with best solution of both worlds
- Virtex-II Pro The First Programmable System To Enable True Architectural Synthesis:
  - Unique bandwidth between embedded processors and HW
  - Unique on-chip solution provides an application-specific mix of logic, memory, integrated processors, and high bandwidth I/O

Technology Transfer at CERN and the LHC developments

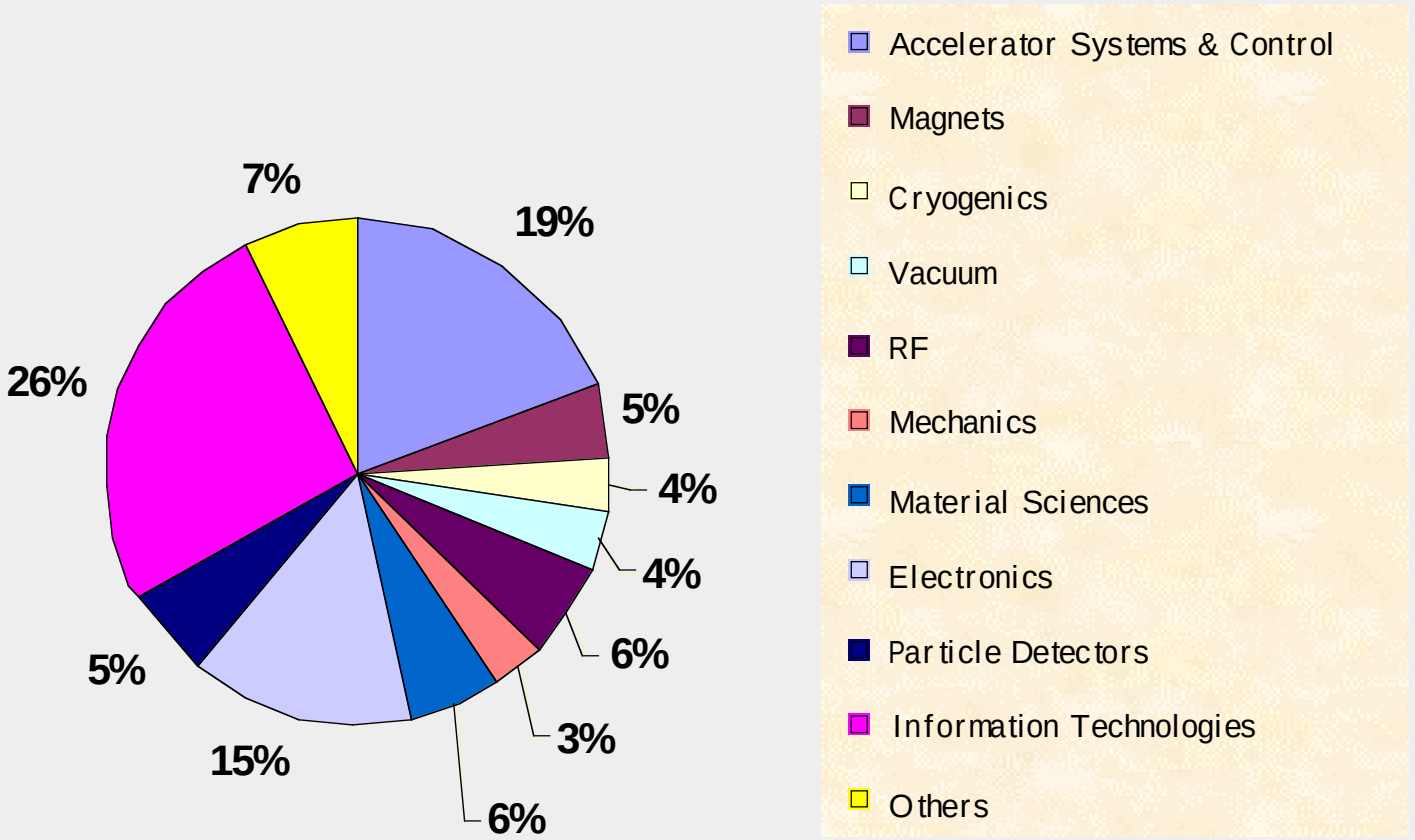
LECC 2002

Colmar, 3 September 2002

presented by S.R.Amendolia/ETT

(thanks for many slides and for help to the courtesy of H.F.Hoffmann, J.A.Rubio, A.Fucci, J.M.Le Goff and the TT Group)

Distribution of Technologies listed in the Database



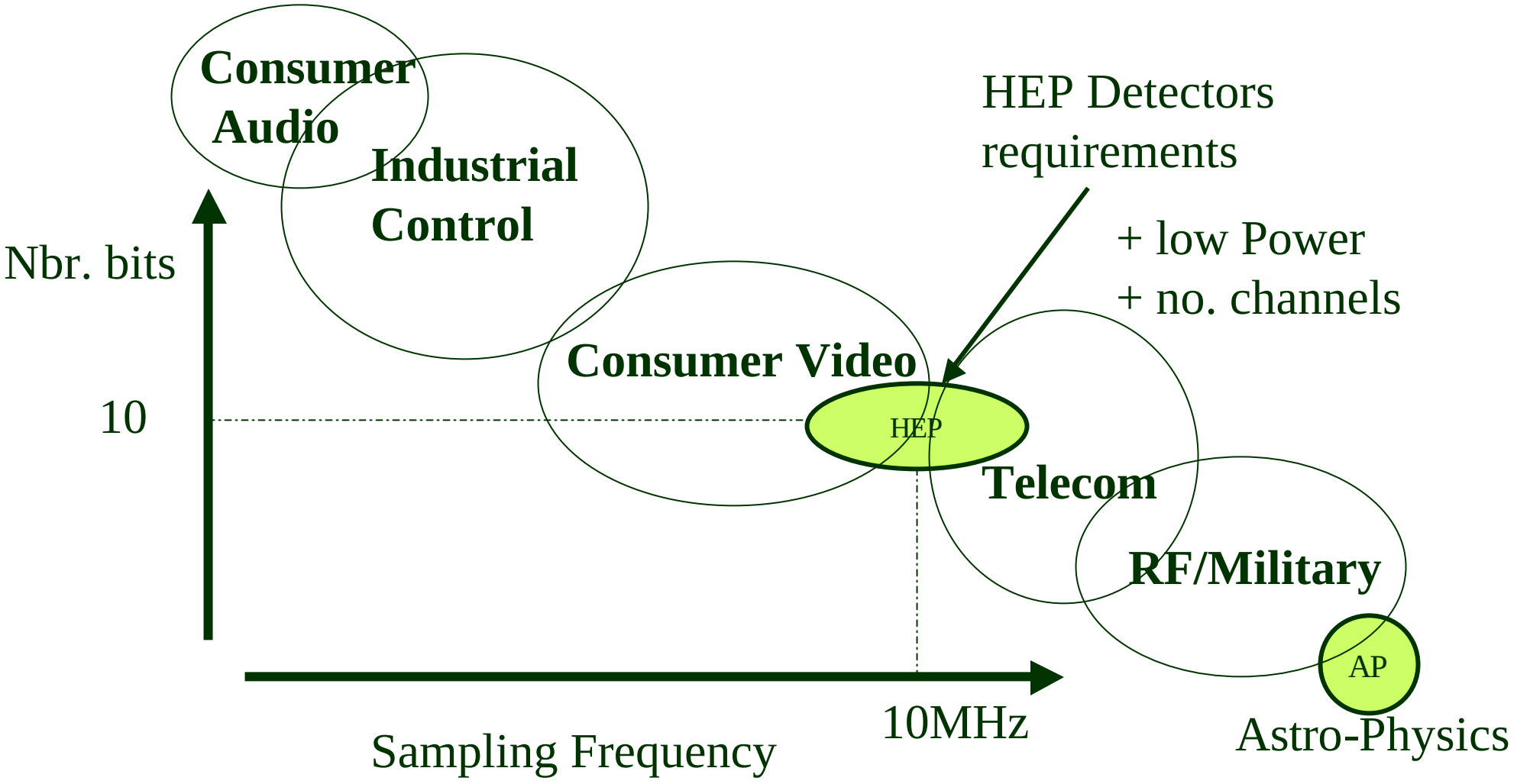
160 technologies are currently listed in the Technology Transfer Database

« Trends in high speed, low power Analog to Digital converters »

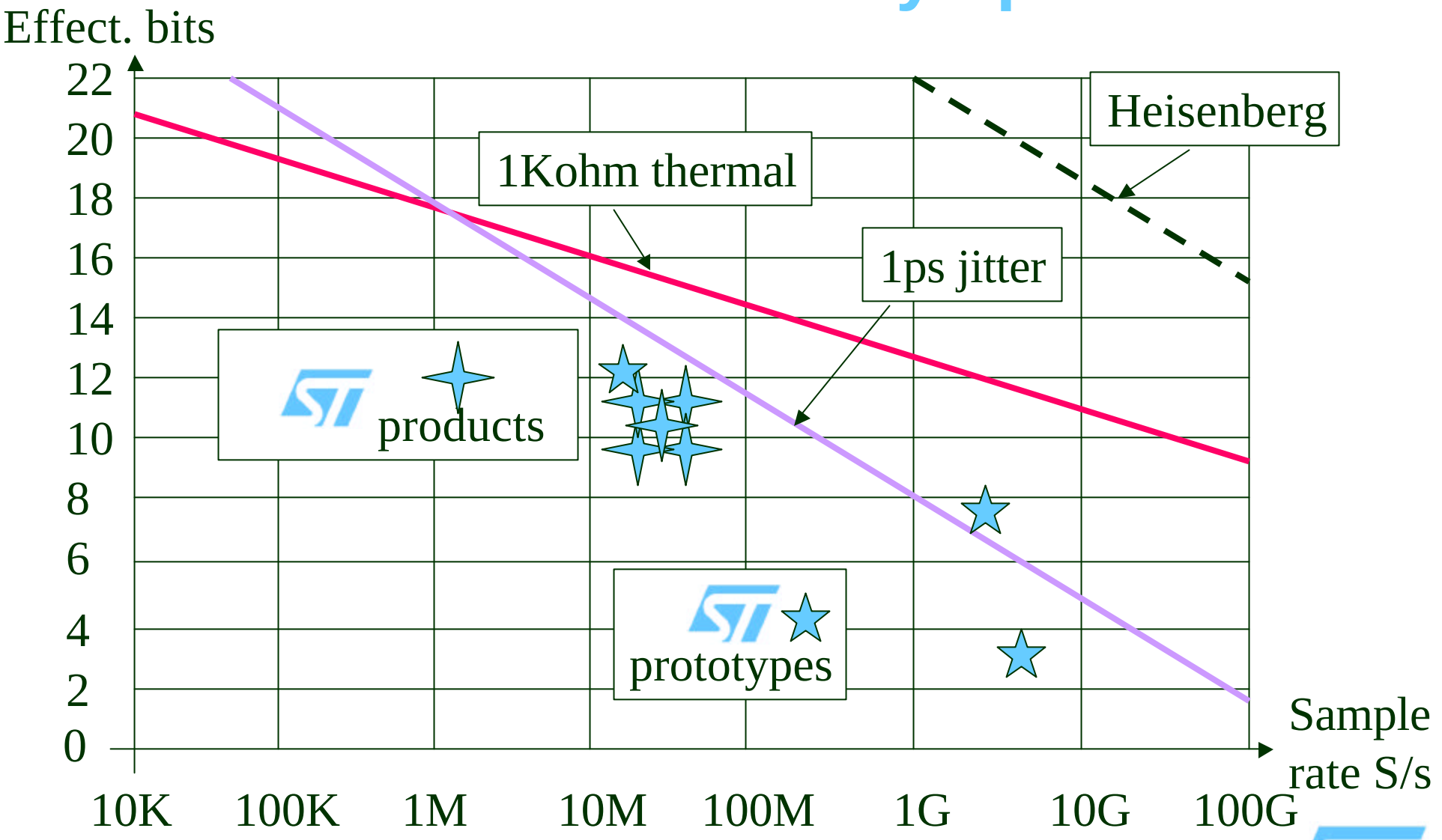
Laurent Dugoujon
Data-Converters Design Mgr.

STMicroelectronics

Hi-volumes & Hi-tech Applications



ST ADCs Accuracy/speed



Parallel Session

- **SESSION A**
  - Electronics for Trackers
  - Data Links, Power System
  - Testing and Quality Assurance
- **SESSION B**
  - Trigger Electronics
  - Data Acquisition
  - Electronics for Calorimeter/Electronics for Muons

Trigger Electronics

- **The ATLAS Level-1 Muon to Central Trigger Processor Interface (MUCTPI)**
  R. Spiwoks (CERN)
- **Tests of the CMS Level-1 Regional Calorimeter Trigger Prototypes**
  W.H. Smith (University of Wisconsin)
- **The Sector Logic Implementation for the ATLAS Endcap Level-1 Muon Trigger**
  R. Ichimiya (Kobe University)
- **Results of a Sliced System Test for the ATLAS End-cap Muon Level-1 Trigger**
  H. Kano (ICEPP, University of Tokyo)
- **Level 0 trigger decision unit for the LHCb experiment**
  R. Cornat (LPC Clermont-Ferrand (IN2P3/CNRS)
- **Pile-Up Veto L0 Trigger System for LHCb using large FPGA's**
  L..W. Wiggers (NIKHEF Amsterdam)
- **Prototype Cluster Processor Module for the ATLAS Level-1 Calorimeter Trigger**
  G. Mahout (University of Birmingham)
- **The Design of the Coincidence Matrix ASIC of the ATLAS Barrel Level-1 Muon Trigger R. Vari (INFN Roma)**

Tests of the CMS Level-1 Regional Calorimeter Trigger Prototypes

W.H.Smith, P. Chumney, S. Dasu,
M. Jaworski, J. Lackey, P. Robl,
Physics Department, University of Wisconsin,
Madison, WI, USA

8th Workshop on Electronics for LHC Experiments

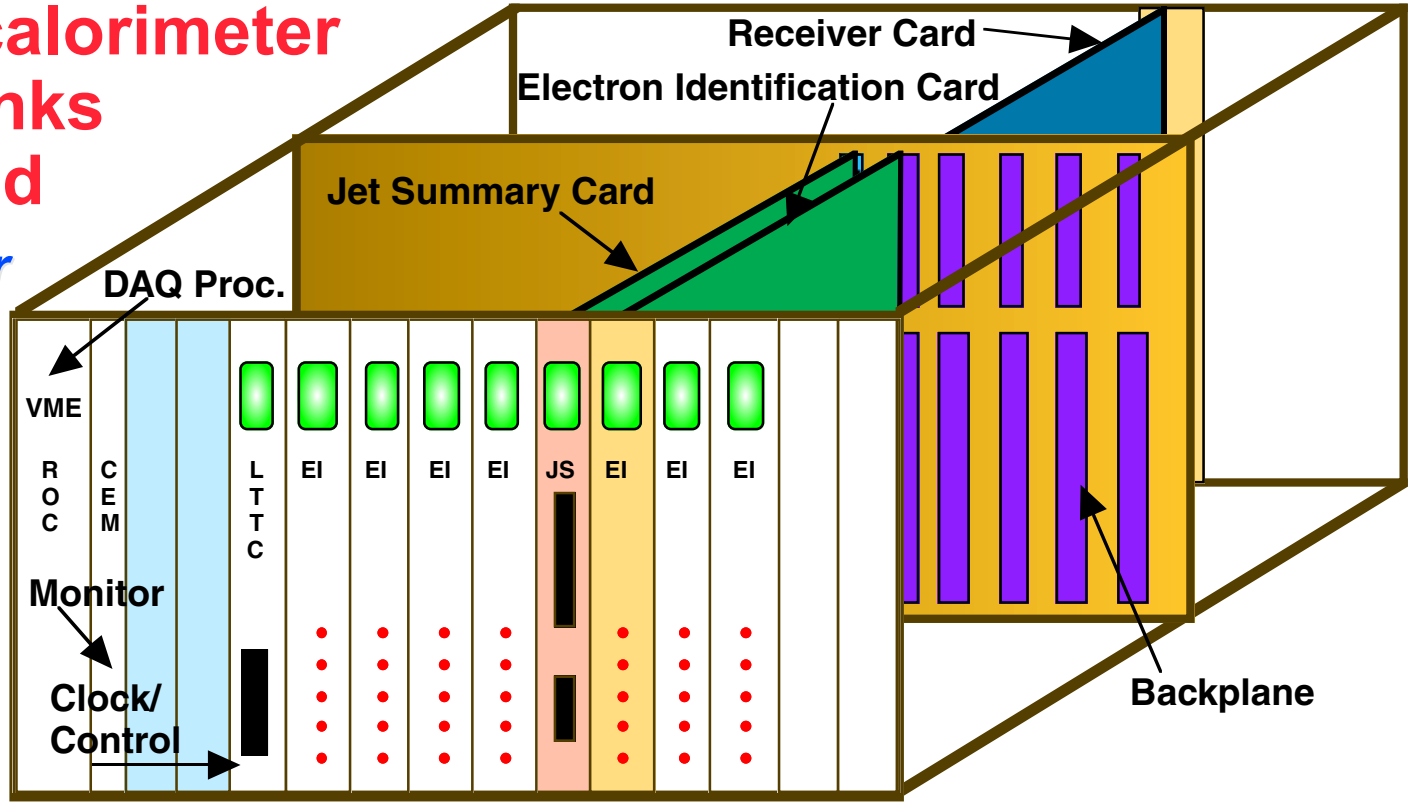
September 10, 2002

The pdf file of this talk is available at:
http://cmsdoc.cern.ch/~wsmith/LECC02talk-wsmith.pdf
See also CMS Level 1 Trigger Home page at
http://cmsdoc.cern.ch/ftp/afscms/TRIDAS/html/level1.html

Calorimeter Trigger Crate

Data from calorimeter FE on Cu links @ 1.2 Gbaud

- *Into 126* rear Receiver Cards*
- *Prototype tested w/ ASICs*

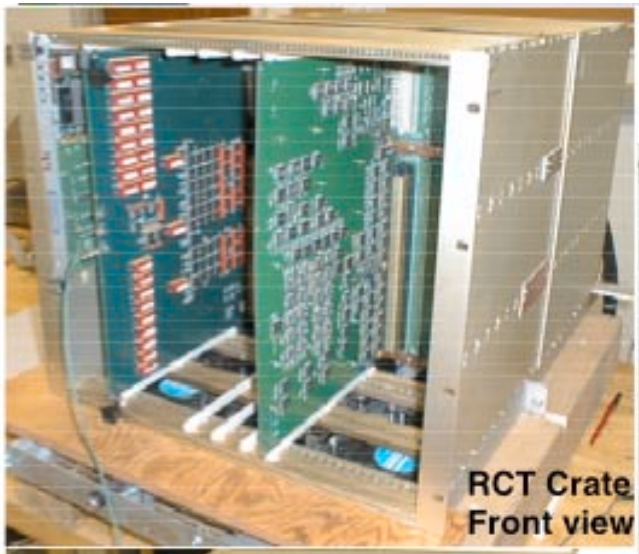


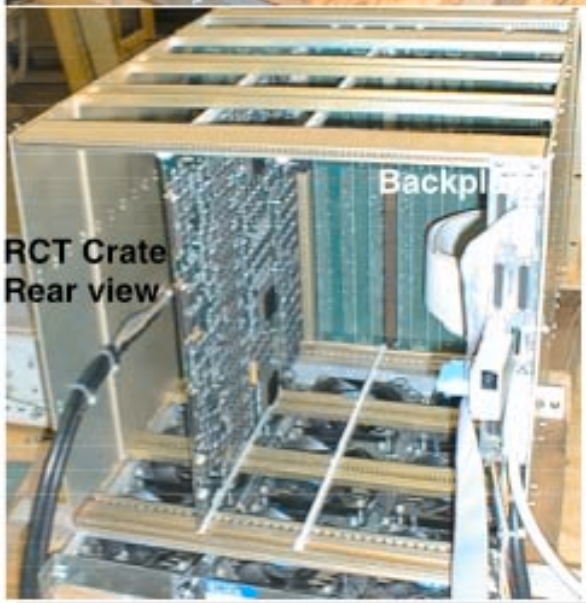
160 MHz point to point backplane (proto. tstd.)

- **18 Clock&Control (proto. tstd.), 126 Electron ID (proto. tstd.), 18 Jet/Summary Cards -- all cards operate @ 160 MHz**
- **Use 5 Custom Gate-Array 160 MHz GaAs Vitesse Digital ASICs**
  - Phase, Adder, Boundary Scan, Electron Isolation, Sort (manufactured)

**Spares not included*

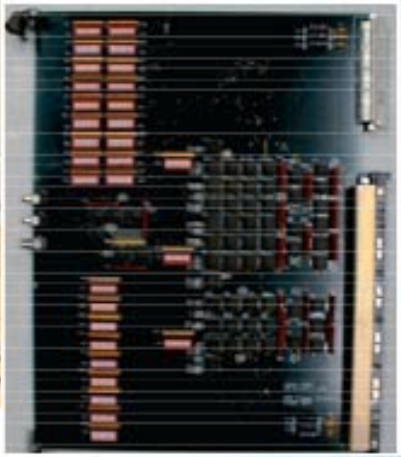
First Generation Prototypes

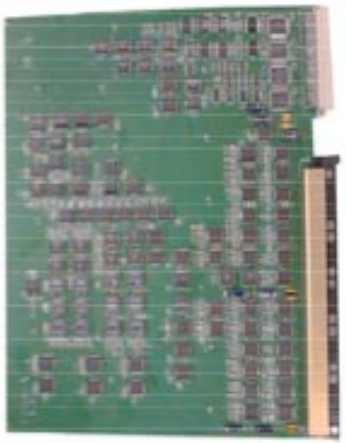




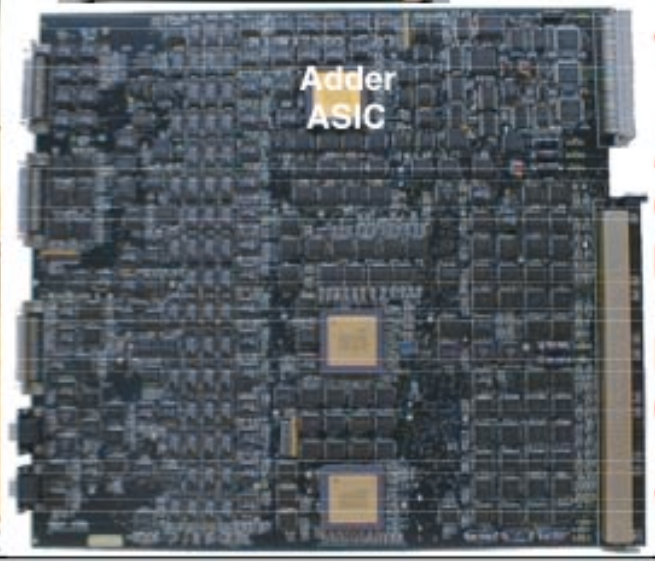
Electron ID Card→

Clock & Control Card





Receiver Card ↓



All Tests Passed

Intercrate sharing checked

Timing checked

Adder ASIC fully qualified for production

Full 160 MHz dataflow verified

VME checked

Conclusions

Conducting second generation prototype tests

- **Crate, Backplane, CCC, RC, Receiver Mezzanine Card, Phase & Boundary Scan ASICs under test -- results good**
  - Phase ASIC validated & production complete
  - Adder ASIC already validated & production complete
- **Serial Link Test Card & Transmitter MC tested & in production**
- **Electron Isolation Card & EISO & SORT ASICs under test**
  - Sort ASIC Validated & production complete

Goals for 2002/3

- **Completion of prototype tests, validate last two ASICs**
- **Integrate Serial Links w/ECAL, HCAL front-ends**
- **Prototype Jet/Summary card manufacture**
  - Ready for manufacture -- waiting for other board tests
  - Integrated HF into this card -- no need for separate HF crate
- **Begin System Production & Test**

The Front-End Driver Card for the CMS Silicon Strip Tracker Readout

8th Workshop on Electronics for LHC Experiments Colmar

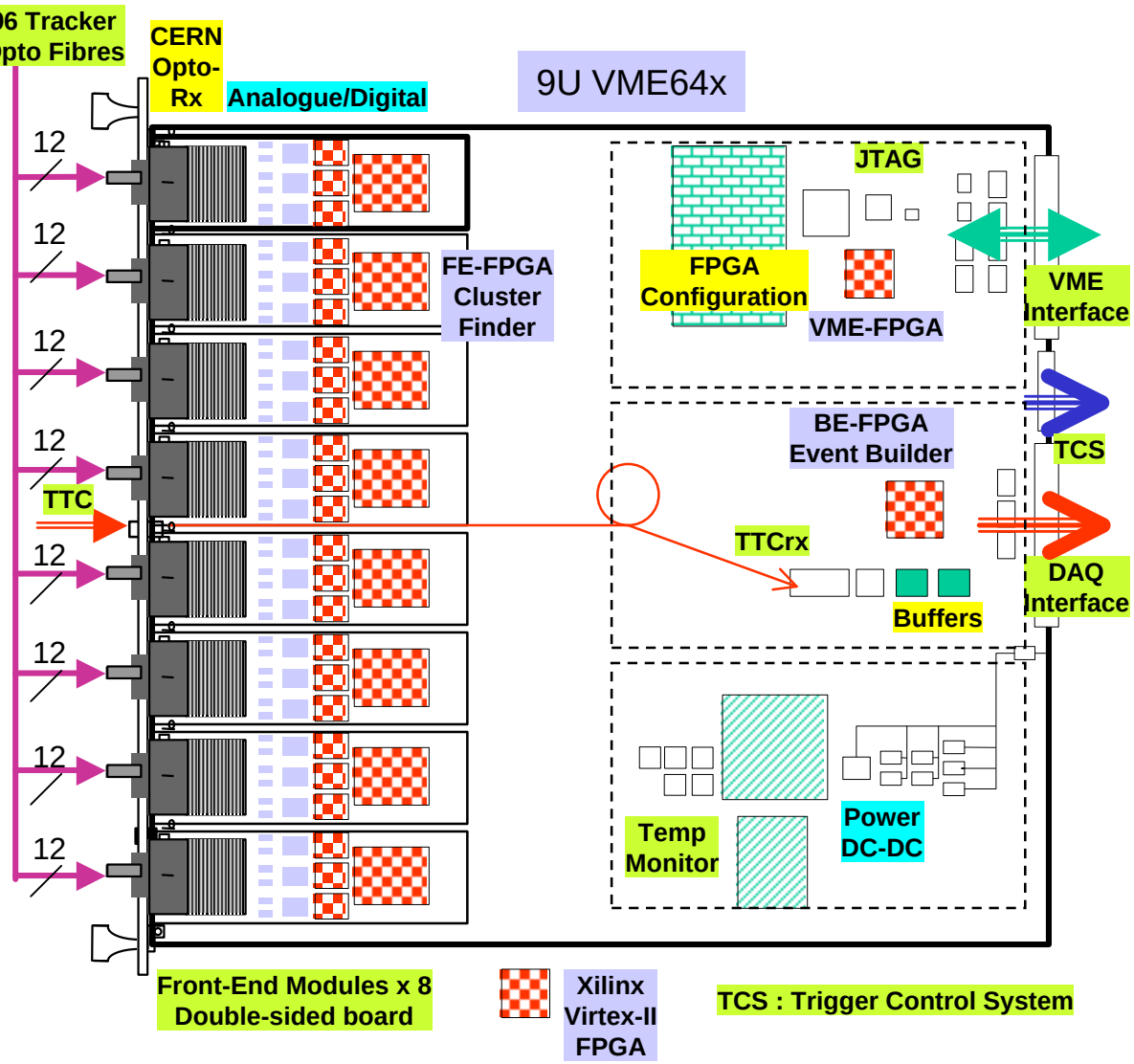
S.A.Baird, K.W.Bell, J.A.Coughlan, C.P.Day, E.J.Freeman, W.J.F.Gannon, R.N.J. Halsall, J.Salisbury, A.A.Shah, S.Taghavirad, I.R.Tomalin
CLRC Rutherford Appleton Laboratory

E. Corrin, C.Foudas, G.Hall
Imperial College London

Presented by John Coughlan
j.coughlan@rl.ac.uk

CMS Silicon Strip Tracker FED

FED Layout



Digital Processing

Flexible Digital Logic:

Xilinx Virtex-II FPGAs 40K->3M gates*

*some in pin compatible packages

Features:

Dual Ported Block Rams

Digital Clock Managers DCM

Double Data Rate I/O DDR

Digitally Controlled Impedance I/O

Various I/O signal standards

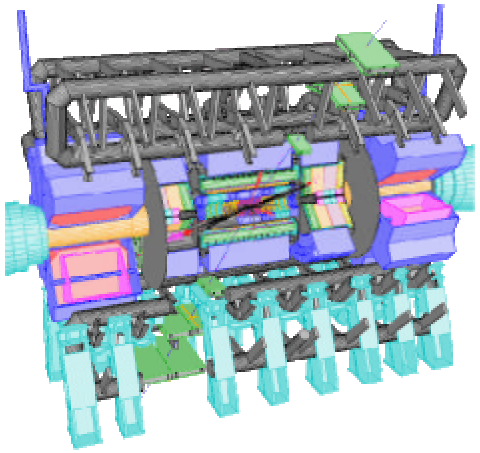
Debugging: Logic Analyser cores

FPGAs programmed in

VHDL & VERILOG

Electronics for Calorimeter/Muons

- **A Configurable Radiation Tolerant Dual-Ported Static RAM macro, designed in a 0.25 µm CMOS technology for applications in the LHC environment**
  K. Kloukinas (CERN)
- **Overview of the new CMS electromagnetic calorimeter electronics**
  P. Busson (Laboratoire Leprince-Ringuet, Palaiseau)
- **Front-end Electronics for the LHCb preshower**
  R. Cornat (LPC Clermont-Ferrand (IN2P3/CNRS)
- **A BiCMOS Synchronous Pulse Discriminator for the LHCb Calorimeter System D. Gascón (Barcelona University)**
- **Channel Control ASIC for the CMS Hadron Calorimetry Front End Readout Module**
  R. Yarema (Fermilab, Batavia)
- **A low-power high dynamic range front-end ASIC for imaging calorimeters Maria Grazia Bagliesi (University and INFN, Siena)**
- **ATLAS/LAR Calibration system**
  N. Seguin-Moreau (Laboratoire de l'Accélérateur Linéaire,Université Paris-Sud)
- **Chamber Service Module (CSM1) for MDT Pietro Binchi (University of Michigan)**



ATLAS

CALIBRATION BOARDS FOR THE LAr CALORIMETERS

N. Dumont-Dayot, M. Moynot, P. Perrodo, G. Perrot, I. Wingerter-Seez
Laboratoire d'Annecy-Le-Vieux de Physique des Particules
IN2P3-CNRS
74941 Annecy-Le-Vieux, France

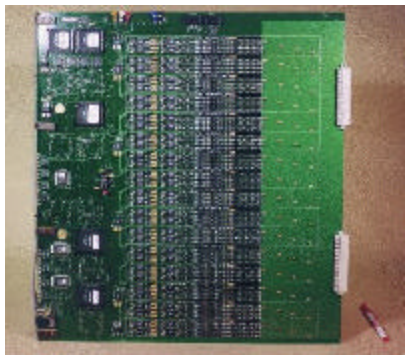
C. de La Taille, J.P. Richer, *N. Seguin-Moreau*, L. Serin
Laboratoire de l'Accélérateur Linéaire,
Université Paris-Sud – B.P. 34
91898 Orsay Cédex, France

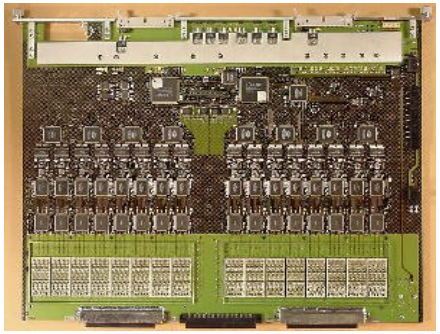
K. Jakobs, U. Schaefer, D. Schroff
Institut für Physik Universität Mainz
Mainz, Germany

ATLAS Lar EM calorimeter readout

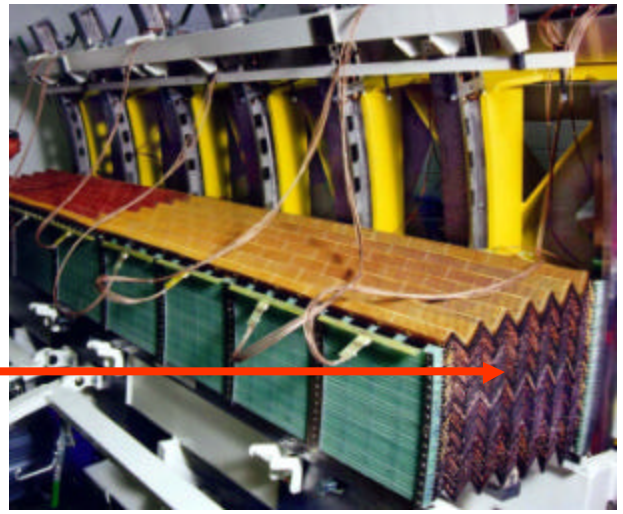
Calibration :
116 boards @ 128 ch

Front End Board (FEB) :
1524 boards @ 128 ch

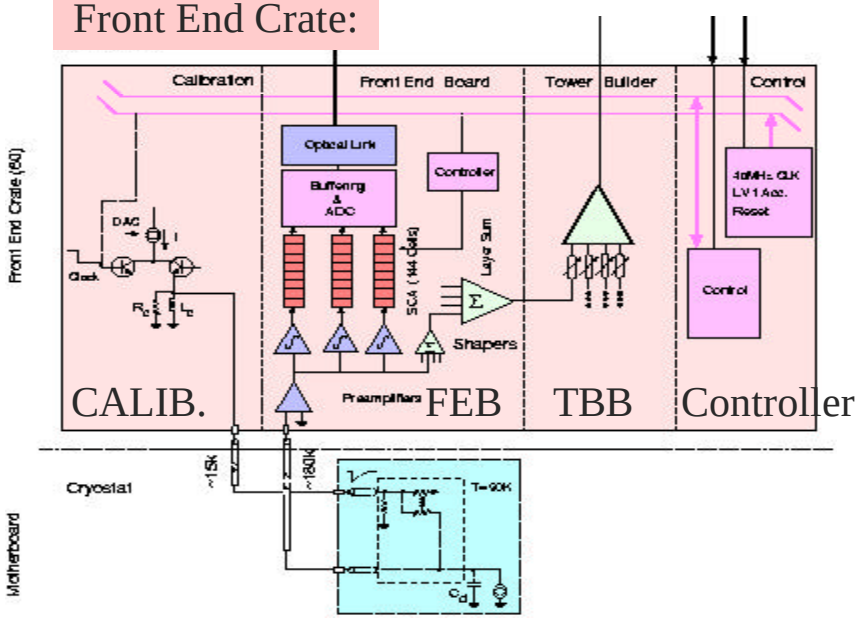




Electrodes



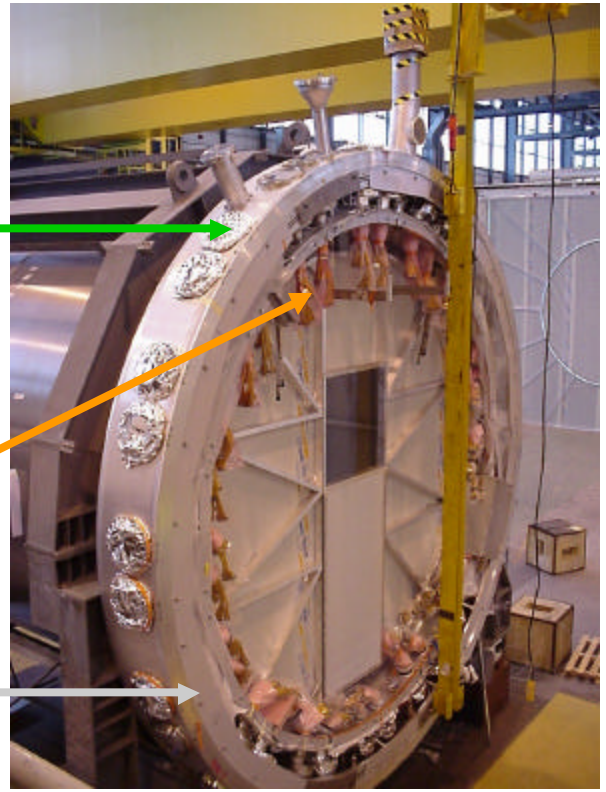
Front End Crate:



Cold to warm Feedthrough

Readout and Calib. signals

Cryostat



CALIBRATION: Requirements and Principle

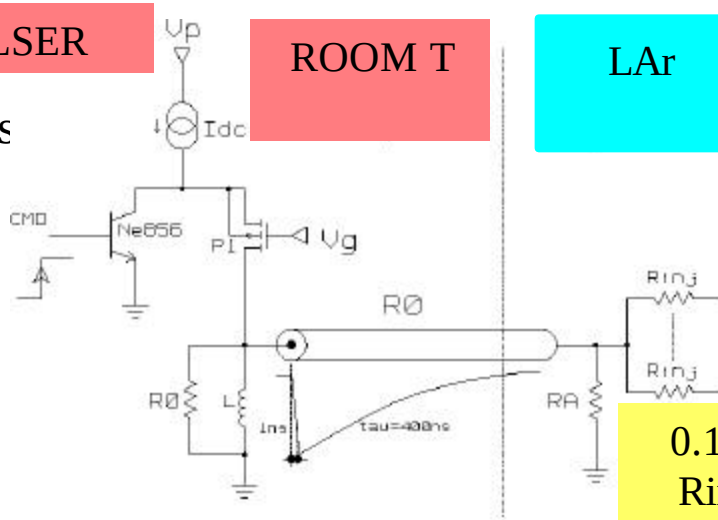
- Goal: Inject a precise current pulse [Ical] as close as possible as the detector pulse
- Rise time < 1ns .
- Decay Time around 450 ns .
- Dynamic range : 16 bits (100 µV to 5V) .
- Integral non linearity < 0.1% .
- Uniformity between channels better than 0.25% (to keep calorimeter constant term below 0.7%)
- Timing between physics and calibration pulse ±1ns
- Operation in around 100 Gauss field
- Radiation hardness:
  - 50 Gy, 1.6 10^{12} Neutrons/cm^2 in 10 years
  - Taking account safety factors, DMILL chips must be qualified up to 500 Gy, 1.6 10^{13} Neutrons/cm^2
- Run at a few kHz

PULSER

ROOM T

LAr

HF SWITCH



0.1%
Rinj

$$Ical = Idc \frac{R0/2}{Rinj} e^{-2R0t/L}$$