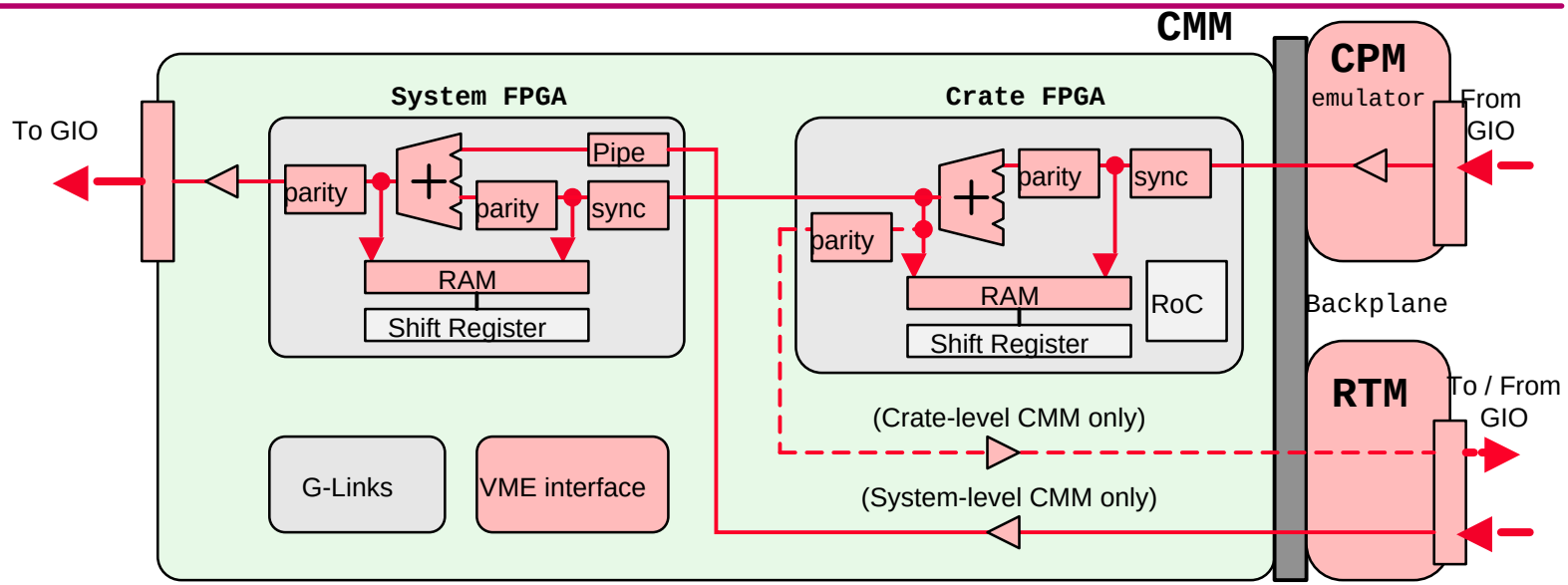
Common Merger Module, Status Report

- Testing the Real-Time Data Path
- Commissioning the FPGA-loading Logic
- Next Design Iteration of CMM
- Summary

Real Time Path Tests



- What we haven't done:
  - not driven >2 channels of data at once
  - no soak tests
  - no testing of readout path
- What we have done:
  - tested all IO channels to/from RTM, CPM & CTP
  - tested complete functional path through module
  - used test patterns designed to expose functional & timing errors

Real-time path tests: Results

- Tests of real-time path now finished:
  - All I/O works, including all backplane input to CMM slot 0
  - No hardware problems found on CMM
    - (other than known broken tracks).
  - Couple of firmware pin-out bugs found & corrected.
- More exhaustive tests should be performed when we have access to the TTC, CTP, 14 CPMs, etc.
- Most of untested real-time logic is within FPGAs, which have been
  - exhaustively simulated in software
  - tested at factory.
- We can therefore allow ourselves some confidence in the real-time logic.

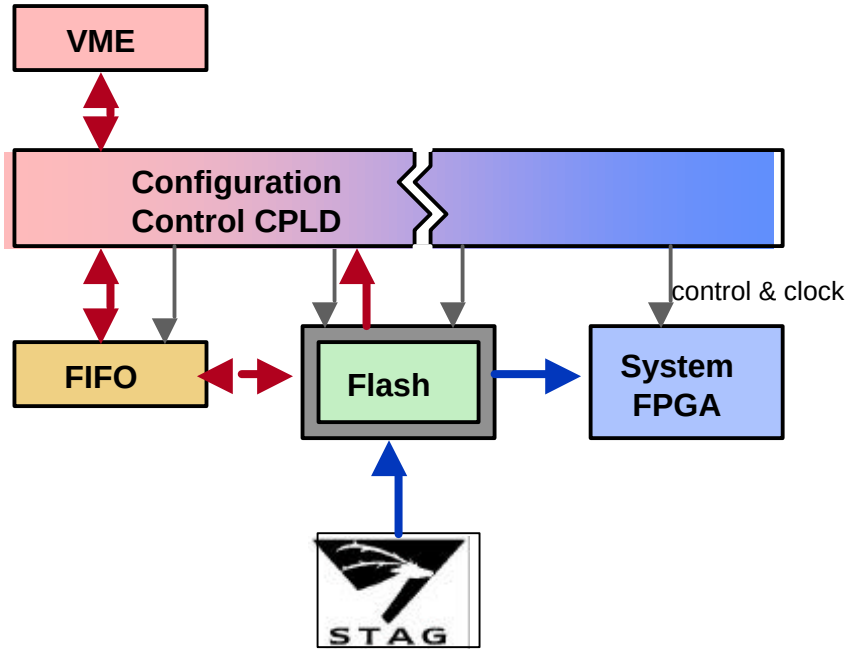
FPGA Configuration: Status

What we can do:

- read & write data VME ? FIFO
- load data FIFO ? Flash
- read data VME ? Flash
  - (few bytes of test data)
- erase Flash from VME
- load data Stag Programmer ? Flash
- programme Flash ? FPGA

Problems so far:

- wrong bit-file options set initially
- Stag temperamental
- problems fitting all required functions into single CPLD
- lacking software to load VME ? Flash



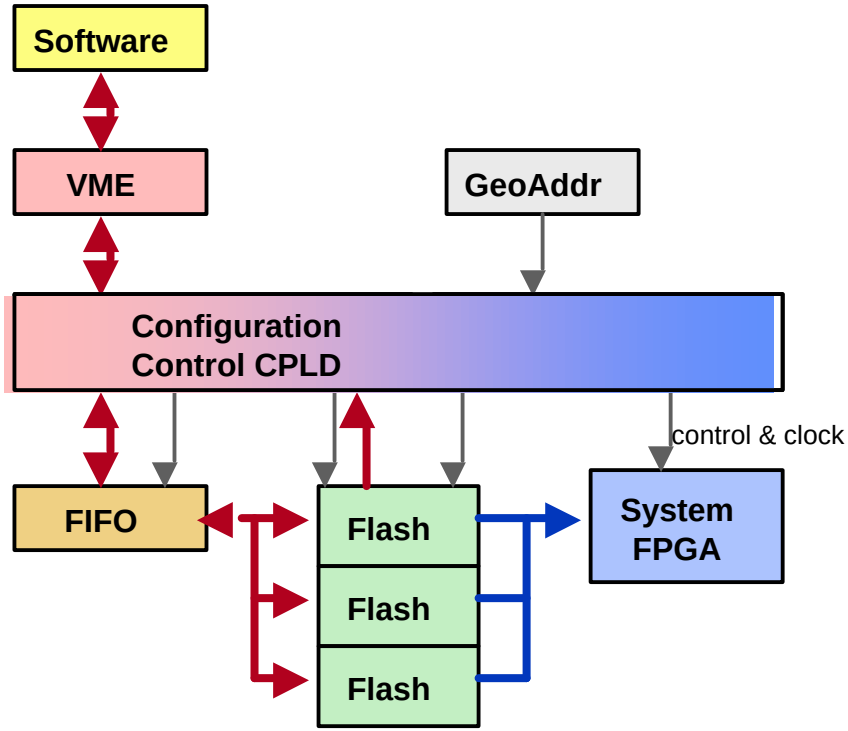
FPGA Configuration: Plans

To do:

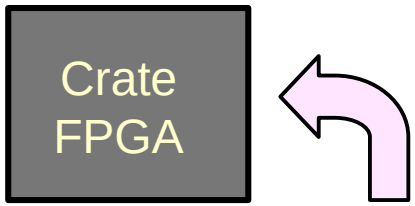
- integrate CPLD design
- produce software

- programme VME? Flash ? FPGA
- load all 3 (System) Flash memories
- Test GeoAddr Logic:
  - determines which bit file is loaded ? FPGA.

- Test Flash memory of correct size:
  - due to miscalculation, current Flash memories are only half the size required.
  - need to hold 2 configurations / Flash; have space for 3.
  - pin-compatible device of required size is available.

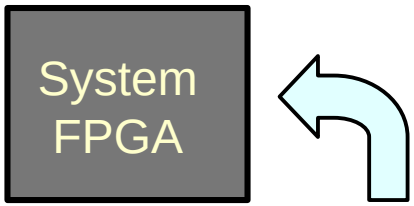


FPGA Configuration Requirements



- CP hit counting:
  - Crate Logic (Crate-CMM version)
  - Crate Logic (System-CMM version)
- Jet hit counting:
  - Crate Logic (Crate-CMM version)
  - Crate Logic (System-CMM version)
- Jet Energy summing:
  - Crate Logic (Crate-CMM version)
  - Crate Logic (System-CMM version)

- Crate- & System-CMM versions differ w.r.t. pins & parity generation.
  - could do this on board but more flexible to do it in FPGA



- CP hit counting:
  - NULL Logic (Crate-CMM version)
  - System Logic (System-CMM version)
- Jet hit counting:
  - NULL Logic (Crate-CMM version)
  - System Logic (System-CMM version)
- Jet Energy summing:
  - NULL Logic (Crate-CMM version)
  - System Logic (System-CMM version)

- 'Null' files: prevent FPGAs running through init cycle continuously; light LEDs; possibly hold monitoring firmware; allow us to use same config.-control firmware as Crate logic.

(So far we've assumed e/? and ? logic will always be the same).

Future Plans

- Finish commissioning configuration logic
- Update CMM firmware to new readout data spec.
- Start testing Readout Logic:
  - use DSS to receive G-link
  - bodge L1As
  - test CMM G-link control
  - check data format
  - maybe test with RODs?
- Test with TTC
- Aim: finish these tests by end of December, ready to....

- Start work on next CMM design:
- correct bugs found with current design
- re-work VME interface:
  - VME CPLD has bottleneck around data bus which makes design mods. difficult.
  - would bigger devices help? (problem is mainly flexibility rather than size)
  - move some logic to other CPLDs & FPGAs?
- Aim: next CMMs ready for slice tests end of March '03.

Summary

- Finished testing real-time logic, successfully
- Making good progress commissioning FPGA-configuration logic
- Some problems placing designs in CPLDs
- About to start testing readout logic using DSS
- Plan to have next iteration of CMMs ready for slice tests in April.