ROD Firmware Updates

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RAL

ROD Modifications

- **All 3 additional designs done**
  - CP CMM
  - JEM Slice
  - JEM Roi
- EEPROM's delivered to R1 lab on 8/10/02
  - Basic tests were done in R25 HDL
  - Require Bruce to test them.

ROD Problem Report 15

- **Created new version of SLINK FPGA, (0x0F), with a smaller data buffer to enable insertion of ChipScope Core.**
- **Created new version (0x13) of ROD CONTROLLER to improve Flow Control.**
- **Need these verified by Bruce before I come over to Lab with ChipScope.**