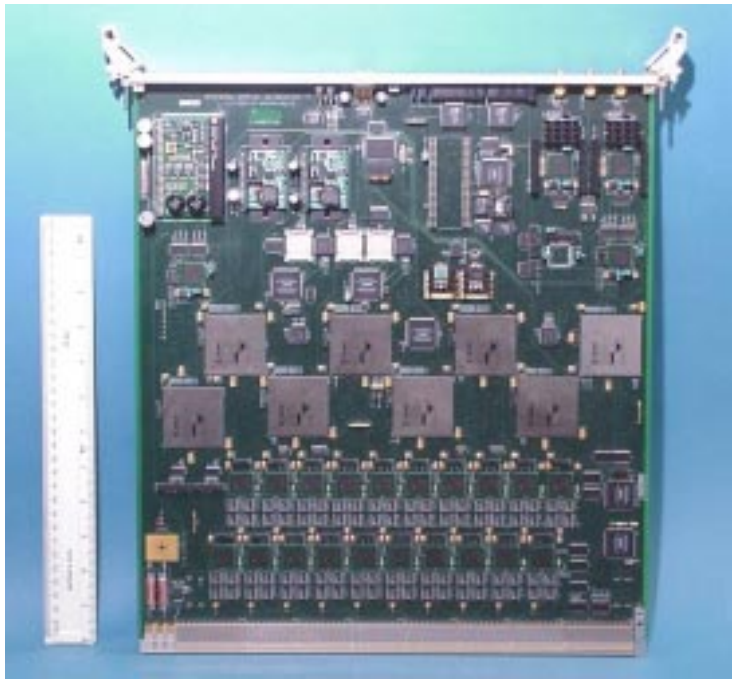
CPM Prototype Hardware + related cards

- Progress
- New Cards
- TTCdec
- LVDS connectors
- Mechanical items
- More testing
- Summary



R. Staley

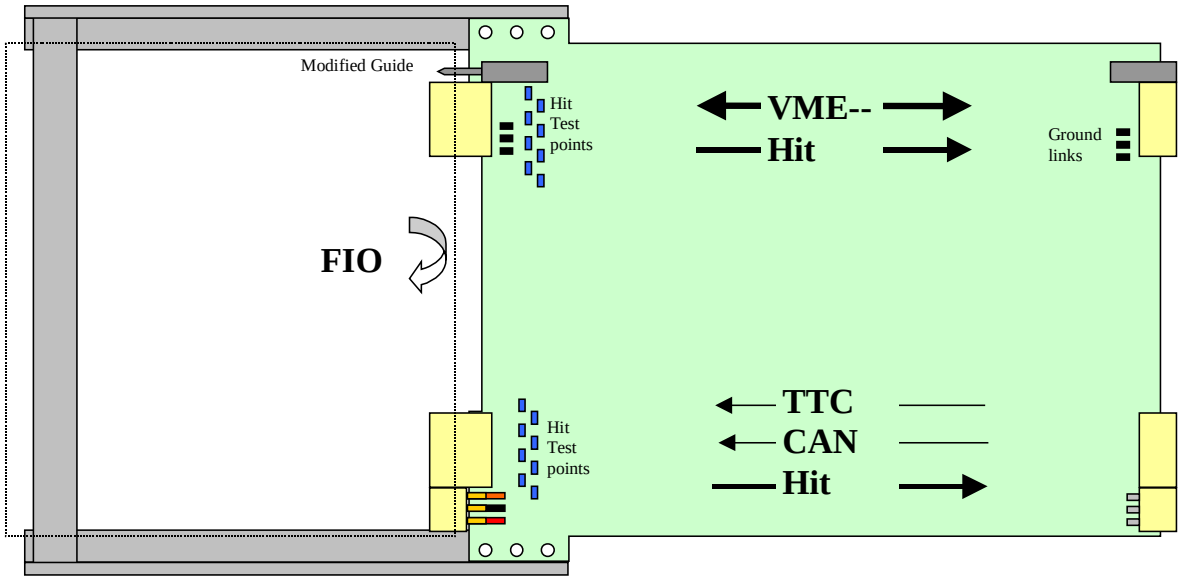
THE UNIVERSITY OF BIRMINGHAM

Progress (since last status report)

- All Serialisers , CP Chips , ROCs and HitSum FPGAs configure from FLASH memory
- Clock Distribution working with TTCdec.
- Onboard 160Mb/s from Serialiser to CP Chip working …(GM.)…

New Cards - Crate Extender

- VME , Hit outputs , TTC and CAN.
- + CMM position.
- Loopback FIO at module connector. All FIO signals.



http://www.ep.ph.bham.ac.uk/user/staley/CPM_Extender.pdf

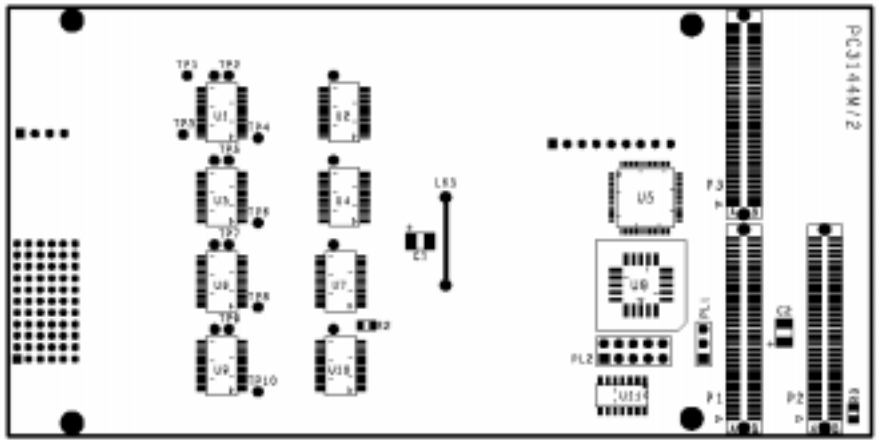
PCB expected 28th October.

R. Staley

THE UNIVERSITY OF BIRMINGHAM

New Cards - LVDS Source for DSS

- New connector to match AMP compact cable assembly.
- Cable pre-compensation R + L.
- JTAG EEPROM.



http://www.ep.ph.bham.ac.uk/user/staley/DSS_LVDS_3_1.pdf

PCB expected 'end' October.

TTCdec

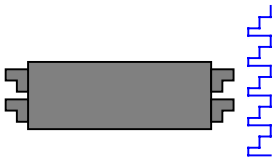
We are using a Version 2.2 TTCrx part.
expected V3.0, but discovered this doesn't exist!

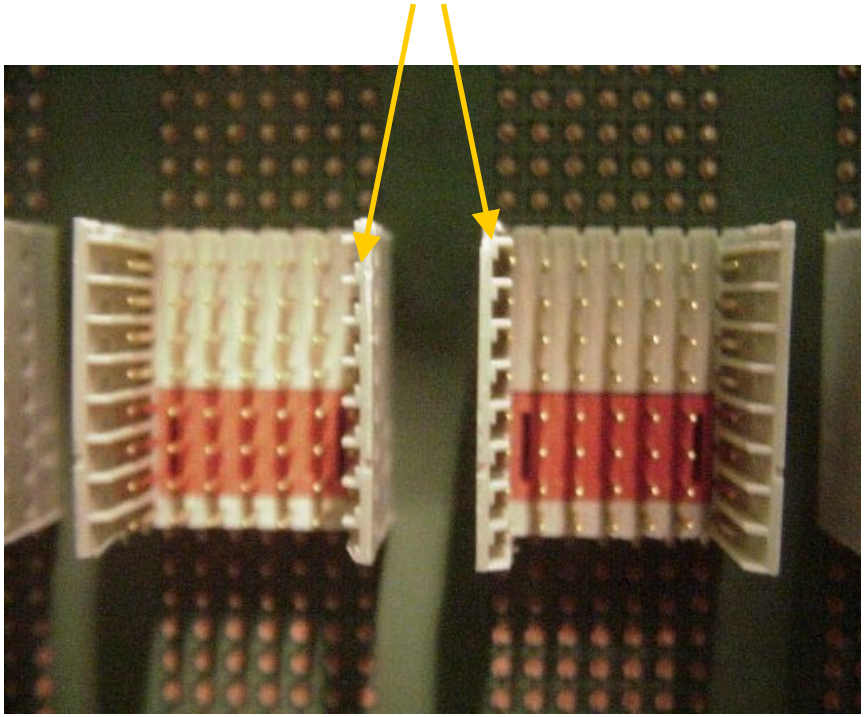
Implications for CPM.

- No I2C → clock phase adjustment using TTC commands
- No Hardwired ID as PROM defines ID. → Geog. Addr ignored
- ERDUMP, CRDUMP and INIT are TTC broadcast commands.

LVDS Cable connectors

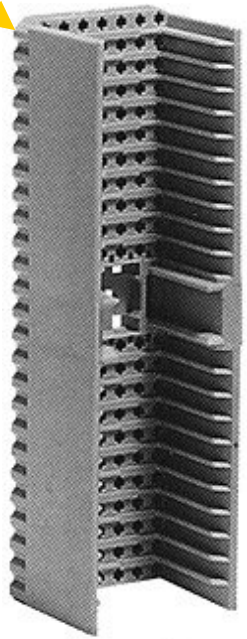
Cables are polarised, but orientation has not been specified.
Cable shrouds can (and have been) placed either way:





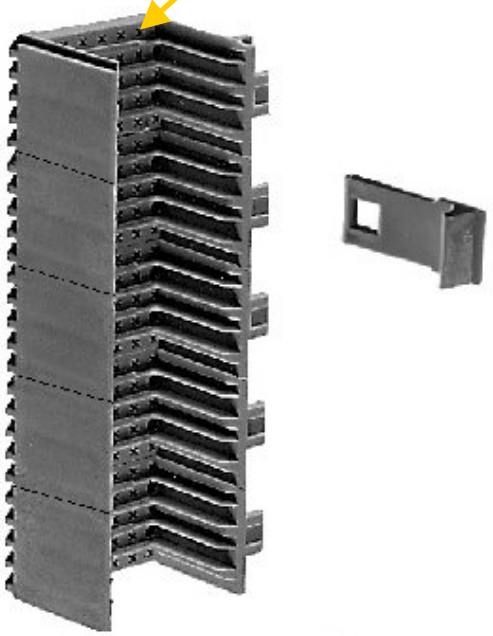
From my AMP catalogue:

a1 (page20)



Type A

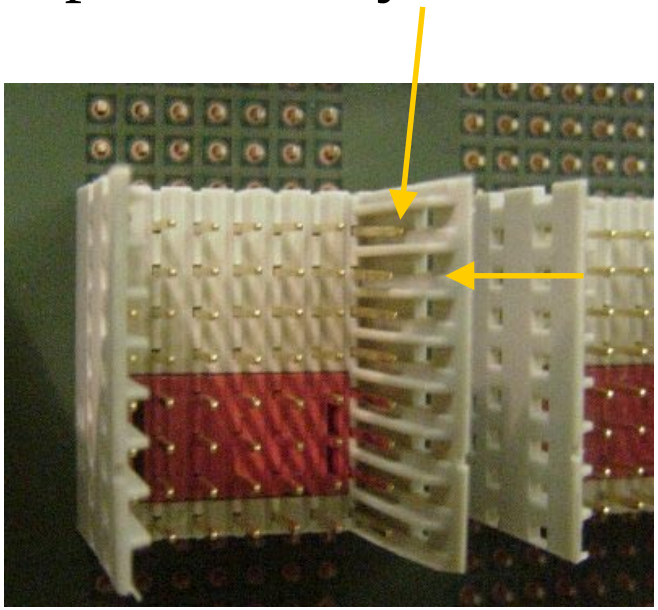
a1 (page48)



R. Staley

THE UNIVERSITY OF BIRMINGHAM

The outer columns of pins (z & f) interfere with the cable connector and become permanently bent:



" Luckily", the cable connectors are held by the jammed pins.

" Fortunately " the cables can be inserted with either orientation.

Mechanical Items

Mechanical Strengthening - Still unresolved.

CP Chip Heatsink - must be removable for rework.

- Clips to BGA
- Clips to PCB , ie:

More Testing …

- LVDS receivers and connection to Serialisers
- Backplane FIO
- Test ROCs and Glink output
- Test Hit Sum FPGAs and output to CMM slot

…

- BERT on 80 LVDS links

…

- CAN uC

Summary

Still making steady progress with development.

- Reliable access to FLASH memory
- FPGA configures from FLASH memory
- TTC system operational

Extender will provide better access to CPM

Cable polarisation needs attention before Slice Tests.