Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference
7th June 2002

Heidelberg:	Ralf Achenbach, Paul Hanke, Karsten Penno
Birmingham:	Gilles Mahout
Mainz:	Uli Schaefer
RAL:	Eric Eisenhandler, Norman Gee, Tony Gillman
Stockholm:	Sam Silverstein

1. Birmingham

Gilles outlined the current status of the CPM test programme at Birmingham. They have added ground pins to the crate power connectors, and are awaiting the longer runners from Stockholm. Operation of the VME-- has been thoroughly checked out, and the problem of overheating of the CAN controller has been solved (intermittent contact to the driving crystal oscillator).

There is a problem with writing data to the Flash RAM, where some random locations fail randomly, and require a second write operation. This happens with two different memories and their separate CPLD controllers, but is not yet understood The controller code simulations look fine, so for the moment the problem has been bypassed by employing the double-write procedure, although it will need to be understood and solved at some point.

Another problem is that the post-configuration DONE signals from the 20 Serialiser FPGAs are unfortunately tied together ("wired-NOR" configuration), so for the initial testing, where for safety only a single Serialiser is being configured, it is impossible to know if its DONE signal has been generated. As the configuration controller code requires the DONE signal before proceeding, the problem is temporarily bypassed by merely defining a fixed number of bytes and not requesting a handshake. As there is a limited number of test points available, a small diagnostic test configuration is also being written, which will generate a clock for simple 'scope verification of correct configuration procedure.

A TTCdec card is now needed to enable operation from the TTC system. This will be supplied from RAL next week.

2. Heidelberg

Paul summarised the continuing progress on the hardware, with the complex 6-layer MCM Test Board, containing also the AnIn daughter-card, ready for loading next week. All the necessary hardware for the MCM tests now exists, and Oliver and Karsten have been working on preparing the software to use it.

Karsten explained that for the VME Test module (mother-board + 2 CMC daughter-cards), there are three Xilinx FPGAs for which firmware is needed, one on each board. On the LVDS daughter-card, the FPGA receives the readout (DAQ slice) data from the MCM and formats them for transfer (via the mother-board) to the Virtex daughter-card and 1 Mbyte S-RAM, controlled by a second FPGA. The mother-board contains the third FPGA, providing VME interfacing to the Virtex daughter-card data via a dual-port memory. The final piece of FPGA firmware should be complete within the next two weeks.

Design of the PPM itself is currently not considered a high-priority item, as essentially all its functionality already exists on the MCM Test Board which will effectively emulate a sub-set of the PPM.

Dominique Kaiser still intends to continue working to slim down the RemFPGA code to fit the existing devices, although he will need remote access to the relevant computer at KIP. Work-around solutions are being considered.

Both Paul and Uli will both attend the Trigger Tower Builder/Driver review at CERN next week.

Paul explained that, because of the floor problem, there was a delay on their move to the new KIP building. Although keys will be available at the end of July, the furniture, etc. will not be installed until August, so they won't finally move in until September.

3. Mainz

Uli reported that they have been continuing to work on the real-time data path through the JEM0.1, and trying to move data through the main processor FPGA. He commented that the FPGA configuration procedure appears somewhat unreliable at present, and they are looking into the problem. He again noted that although they could use a crate/backplane assembly, it was not a priority right now. He felt that the focus in Mainz would be on testing the energy data path, which could be done with a single JEM on the bench, and not yet attempting JEM-JEM communication. There have also been problems with a rather narrow data window for the FIO communication, but this was believed to be solved by the addition of output flip-flops in the FPGAs. However, for inter-JEM communication to be tested it was still possible that the FIO signals might need to be clocked into the main processor FPGA by a separately deskewed clock signal, for which they would need a TTC system. One has been ordered, but will apparently not be delivered to Mainz until November, which may well be too late, so this may be something that Stockholm would take on.

4. RAL

In Viraj's absence, Tony summarised the status of work at RAL. The CMM testing by Ian Brawn continues to progress well, and the most recent step has been to get the data playback mode working correctly.

A further six new ROD modules have been assembled and boundary scanned. This showed up a fault with one module, which needs an FPGA to be reworked. These six RODs will then be thoroughly tested by Eric and Tony in the Physics Group Lab, using a subset of the exhaustive tests carried out by Bruce on the first ROD.

The new firmware for the DSS modules, providing correct memory wrap-around for data playback, has been written.

Two GIO (General-purpose I/O) cards have been assembled and are about to undergo boundary scans.

The Rear Transition Module (RTM) layout has been completed and the design is about to go out for pcb manufacture.

There has been success with getting the CANbus to work, and messages can now be passed from a TCM via the 9U crate backplane and received correctly in a CMM. More work is needed to understand some subtleties of the downloading procedure for the microcontroller code.

5. Stockholm

Sam reported that he is preparing the third crate/backplane assembly for shipping to RAL, which requires making all the necessary modifications (replacing power/ground pins/leads, new module runners, GA0 pin fix, etc). The fourth crate will be similarly modified and shipped to Mainz. Sam reminded us that he still has some transmission measurements to make on the backplane at some point.

The longer card guides have been sent to RAL and will be sent soon to Birmingham.

He has proposed a solution to the CMM addressing (GA0) problem in crates #1 and #2, which involves the simple removal of a single pin from a slot 20 connector. He has already done this successfully on crate #3, and believes that in future it should be possible to replace individual connector pins if they get damaged.

A request was made for the Gerber files for the RAL-designed RTM to be put on the web, once the card has been checked out.

He noted that his students have also been continuing to work on porting the dataflow software to Linux.