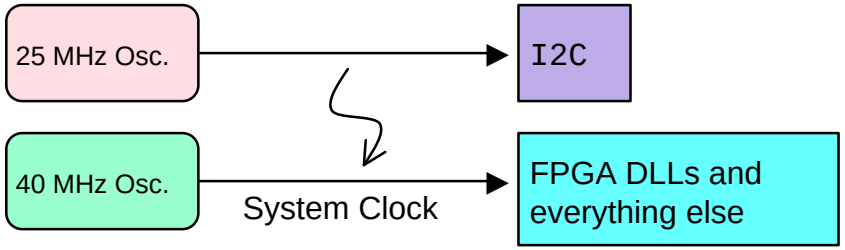
Common Merger Module: Progress & Status

- What we have done since the last meeting.
- Where we are now.

CMM: Clock / DLL problems

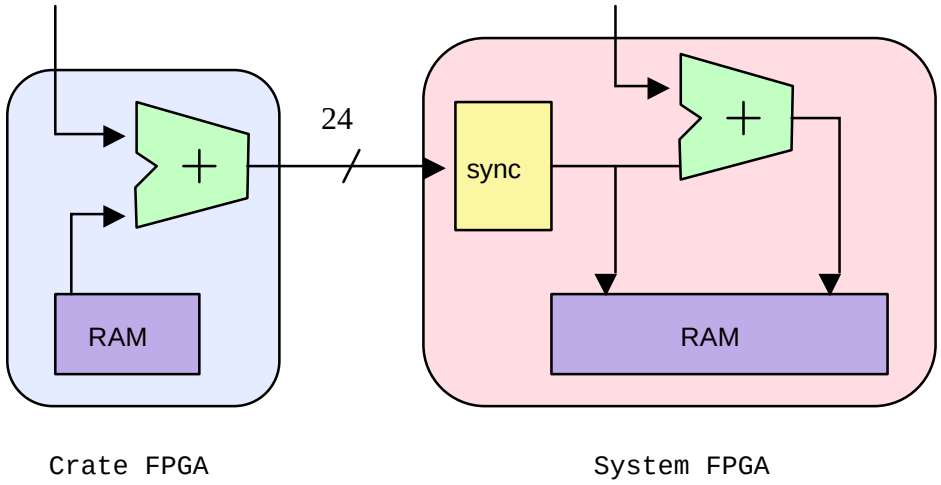
- Previously had problem with DLLs due to upside down RST_DLL signal.
  - Described at last meeting. Solved last month.
- Now found interference between 40 MHz and 25 MHz oscillators, which causes one of FPGA DLLs to loose lock.



- Problem solved temporarily by removing 25 MHz oscillator.
- More permanent solution required:
  - improve shielding?
  - Could I2C use 20 MHz clock (stepped down from 40 MHz)?

CMM: Playback Mode

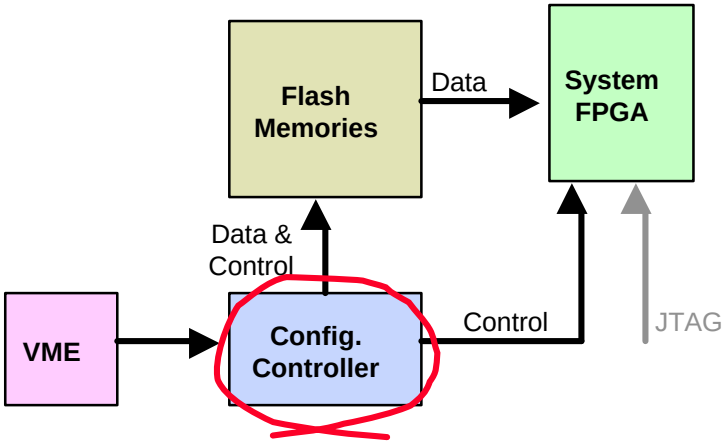
- Data has been transferred successfully from Crate FPGA to system FPGA via real-time data path:



- This required special firmware versions:
  - Crate FPGA that was always in playback mode (so that data in RAM weren't over-written)
  - System FPGA that wrote data from local Crate FPGA to RAM (normally only data from remote CMMs is written to System RAM).

CMM: Other Developments

- Panagiotis has been working on firmware for the configuration controllers, that will allow us to load the System (and Crate) FPGAs from flash memories.



CMM: Current Status & Plans

- The following have been tested and found to work:
  - loading of FPGAs via JTAG
  - DLLs in FPGAs
  - VME interface
  - Playback mode transfer of data Crate ? System FPGA

  - However, none of these tests have been intensive, as we lack software for this.

- Next steps:
  - Test synchronisation logic with incoming data:
    - feed data into CMM via GIO & RTM cards, when available.
  - Get configuration controller working for
    - Flash ? System FPGA.
    - VME ? Flash.
  - Investigate any problem reports transmitted from R1.