CPM Testing

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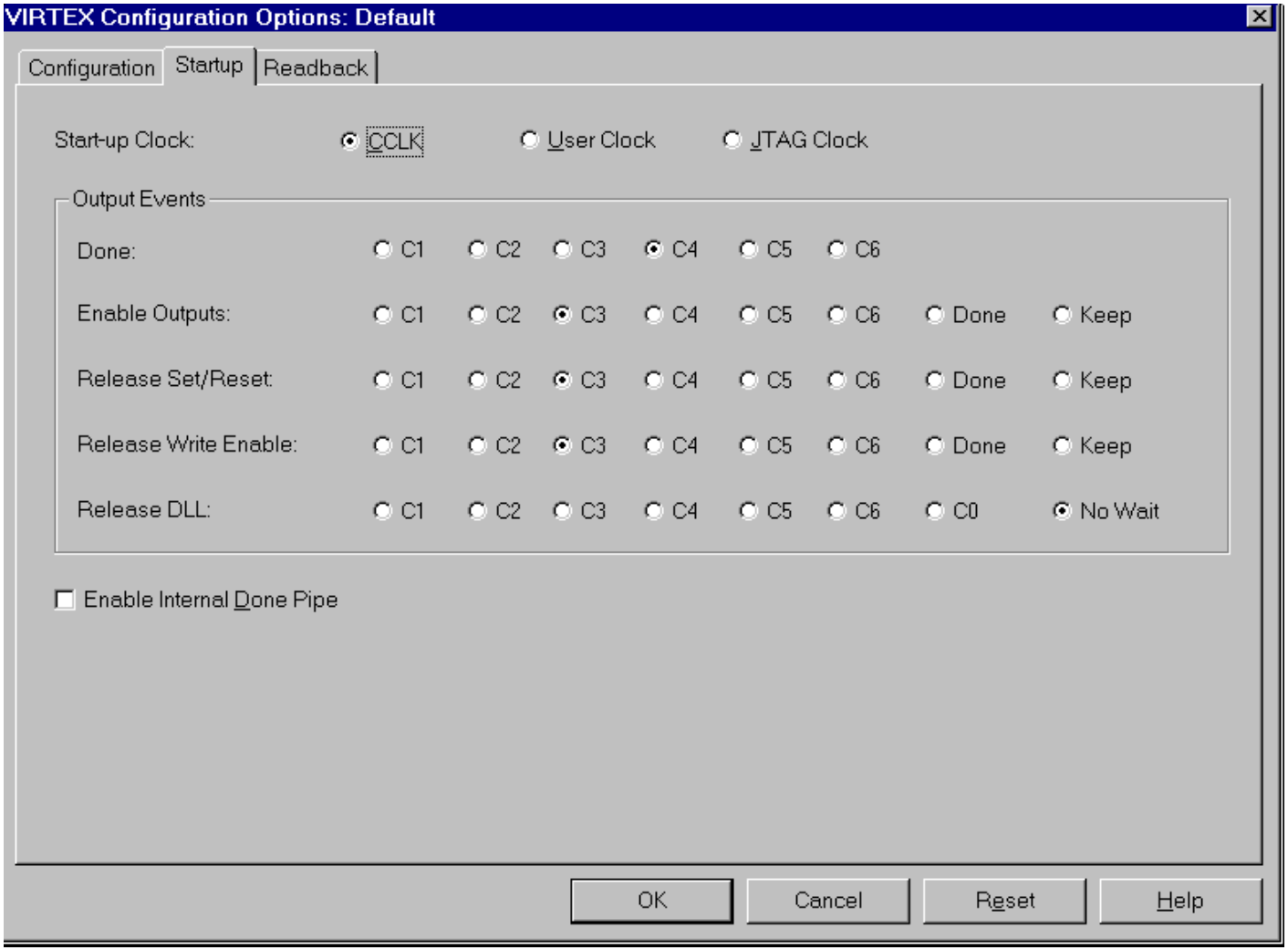
CPM Testing – Problem met

- For safety, decide load only one Fpga: Serialiser V.
- Pb: All Serialisers connected together: wait for DONE signal to be pull up before starting up (I.e: from cfg State to operational state)
- Dummy F/W written to probe status of the Fpga device: recognized pin layout but still refuse start up

Solution: by-passing DONE signal

- Xilinx Alliance give the option to change the start-up sequence in the Bit File: I/Os activated, RAM state changes etc…before DONE signal goes up

Xilinx Alliance Panel



Results: Serialiser successfully loaded.

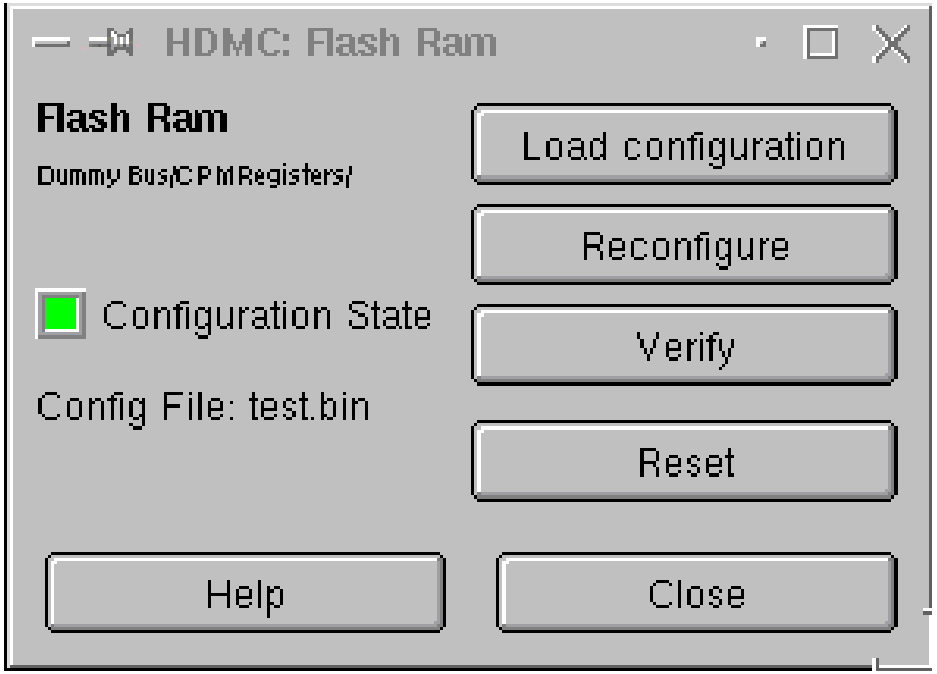
- Step 1: Serialiser V loaded correctly with Dummy F/W : 1 LeD Flashing on Front Panel…
- Step 2: … all the 19 others loaded: 19 LeDs flashing
- Step 3: Downloaded 20 serialisers with their normal configuration:
  - Read a F/W Id of 0000000 …as during the simulation of the Serialiser (must be Ok)
  - R/W to Control Register with no problem
  - DLLs locked
  - Testing Play Back Memory: does not seem to write correctly to the RAM so far…

Fpga Loading: from S/W to H/W

- 1: Design with HDL Pro, Synthesize with Leonardo and create bit file with Xilinx Alliance
- 2: Use HDMC new parts CPFpgaFlashRam to download the F/W bit file just generated inside the Flash Ram
- 3: use VME CR + Mask to download the configuration from Flash Ram to Fpga device

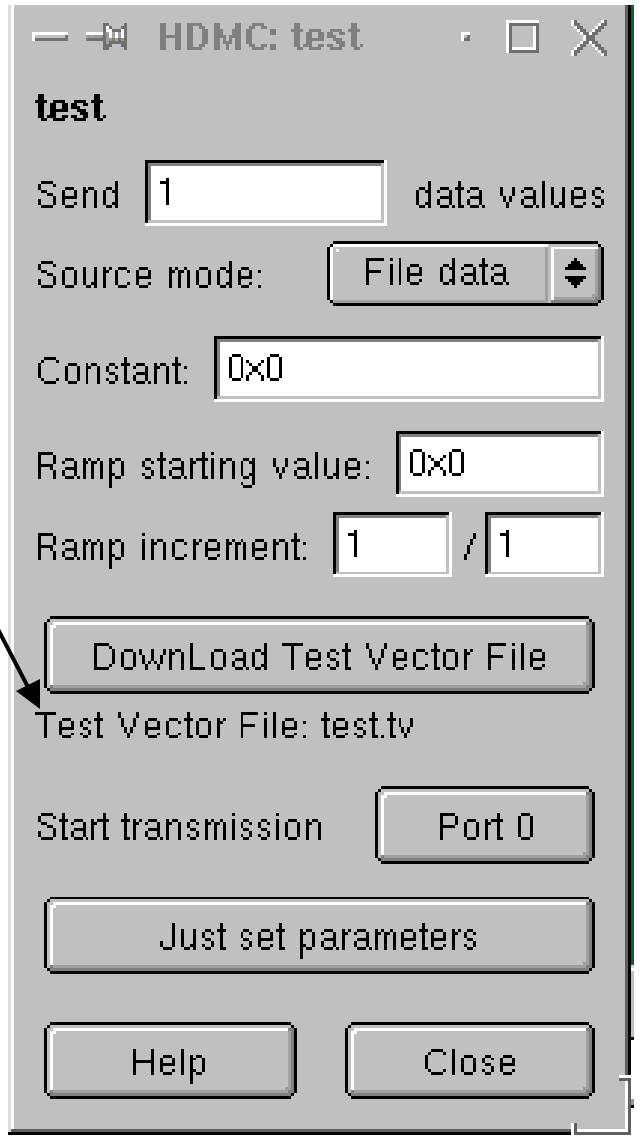
New HDMC Parts: CpFpgaFlashRam

- Ask for Configuration File
- Verify: Read back file from Flash Ram
- Reset: erase Flash Ram
- Bytes are swapped before downloading to take care of the swapped format of the PROM port



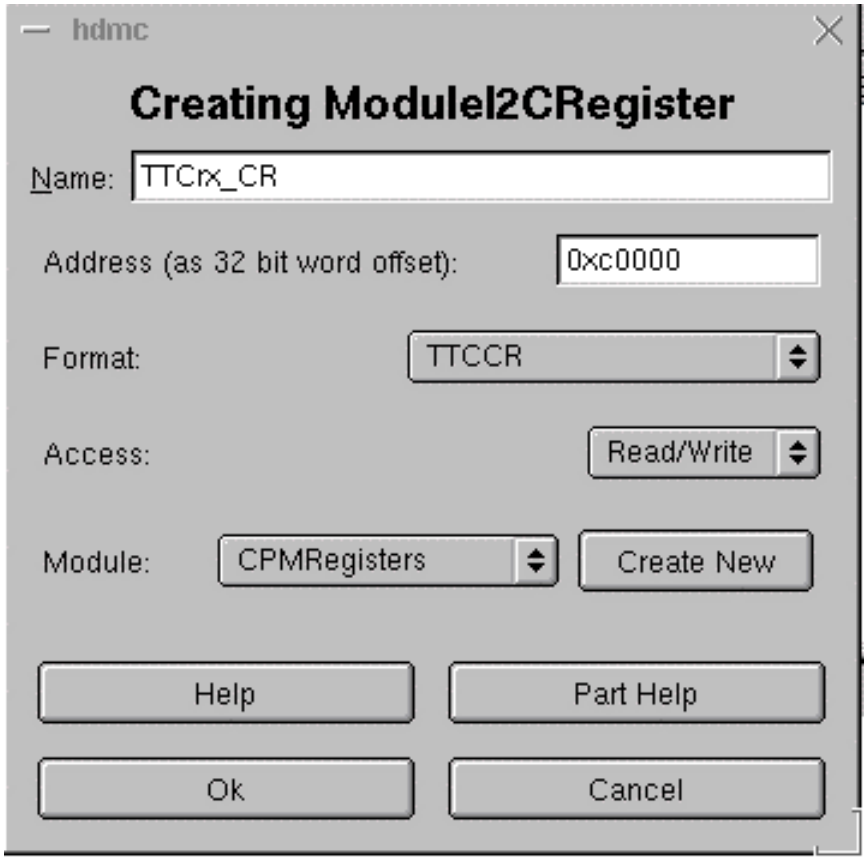
New Part: DataSourceTV

- Load an external file of hex Test Vectors values, to be used inside a RAM for ex.
- CPM application: testing Real Time Path between Srl and CP



Part file, to be done: ModuleI2CRegister

- Read/Write to TTCrx register via I2C access
- Use of only 2 registers to do the access is hidden in the part file and I2C controller
- Four TTCRx registers to be defined: Timing, Control, BncCnt and EvtCnt registers?



Next steps

- One then 7 Cp chips to be downloaded
- Load Memories and play back data
- Check Real Time Data Path + connectivity
- Load and debug others F/Ws: Hit, ROC
- Modules Services of CPM
- TTCrx testing