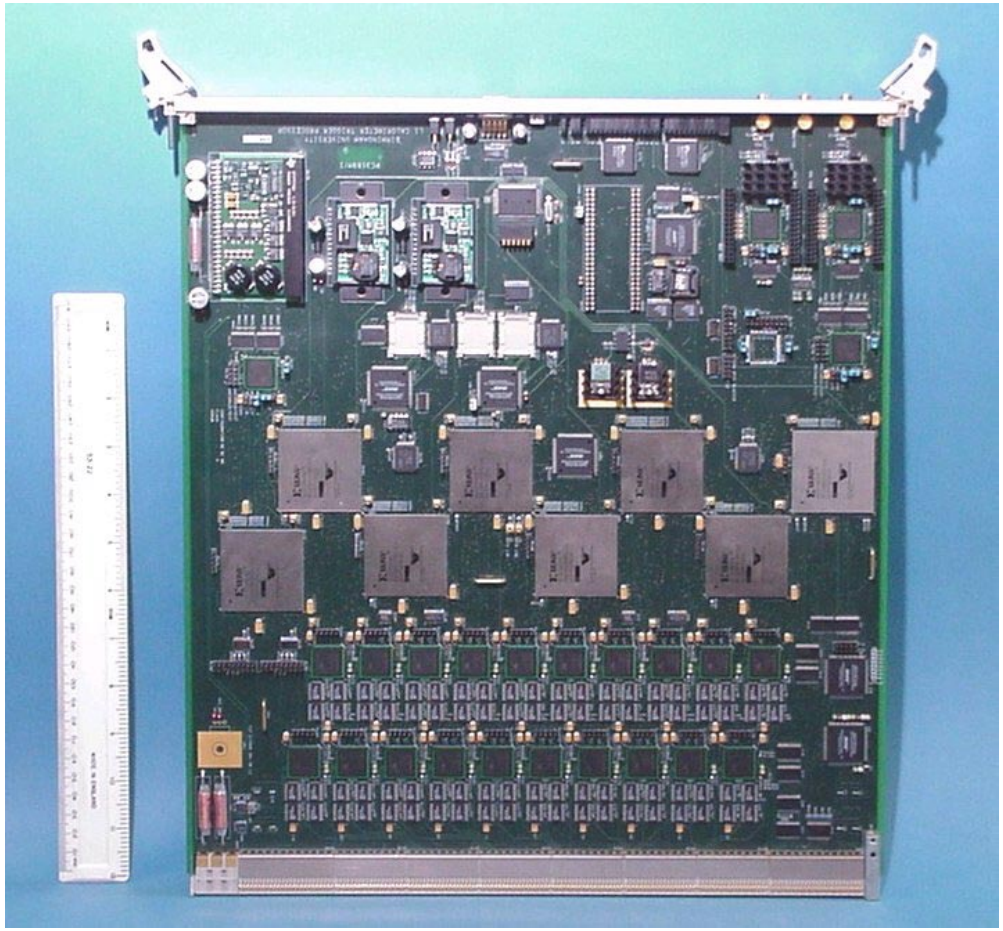
CPM Prototype Hardware

- Documentation
- Progress
- CAN uC
- FPGA Configuration
- Mechanical items
- Next
- Summary



R. Staley

THE UNIVERSITY OF BIRMINGHAM

Documentation

User Guide (Hardware)
http://www.ep.ph.bham.ac.uk/user/staley/CPM_USER.pdf

PCB Modifications
http://www.ep.ph.bham.ac.uk/user/staley/CPM_MODS.pdf

Programming Memory Map
http://www.ep.ph.bham.ac.uk/user/staley/CPM_MM.pdf

R. Staley

THE UNIVERSITY OF BIRMINGHAM

Progress (since last UK meeting)

Clock Distribution with correct PLLs perform as intended.

CAN uC overheating / Geographical Addressing prob. fixed →

VME interface working

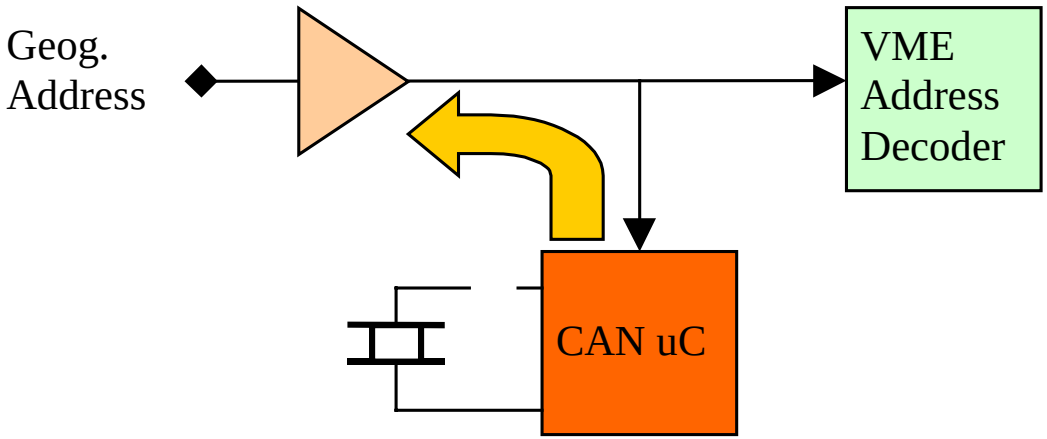
- Access to ID , Revision, Control and Status registers
- R/W and Erase FLASH memory.
- All Serialiser FPGAs configure . →
- Serialisers connected to VME ?

R. Staley

THE UNIVERSITY OF BIRMINGHAM

CAN uC

CAN uC clock oscillator pin was unsoldered , giving an intermittent contact with crystal resonator.
Incorrect operation caused CAN uC to over-heat and also to dump current onto the Geographical Address lines:



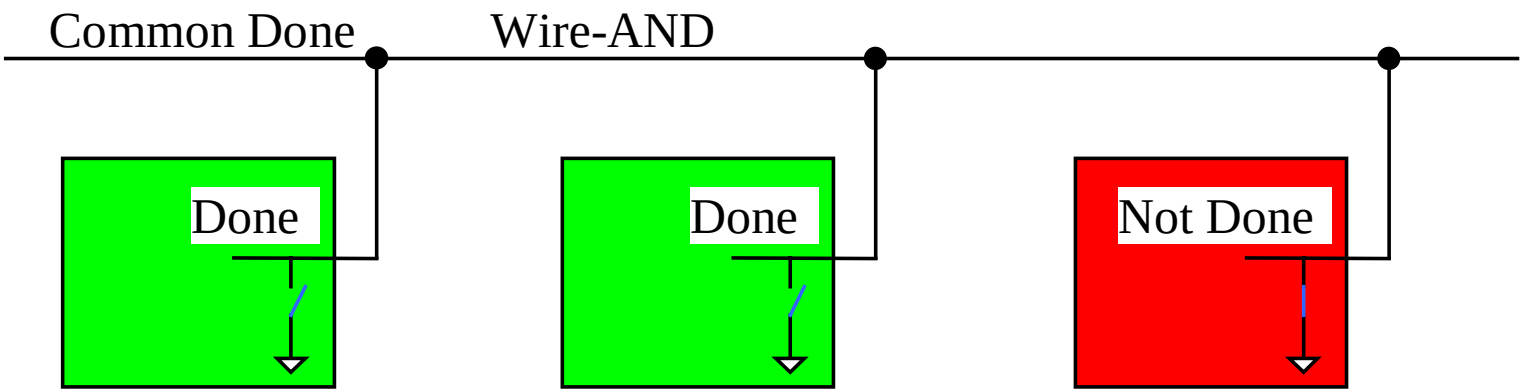
R. Staley

THE UNIVERSITY
OF BIRMINGHAM

FPGA Configuration

XILINX FPGAs signal 'configuration completion' by releasing the DONE pin … and then wait for this pin to be released externally!

On the CPM , groups of FPGAs have their configuration DONE pins tied together (as suggested in various XILINX notes).



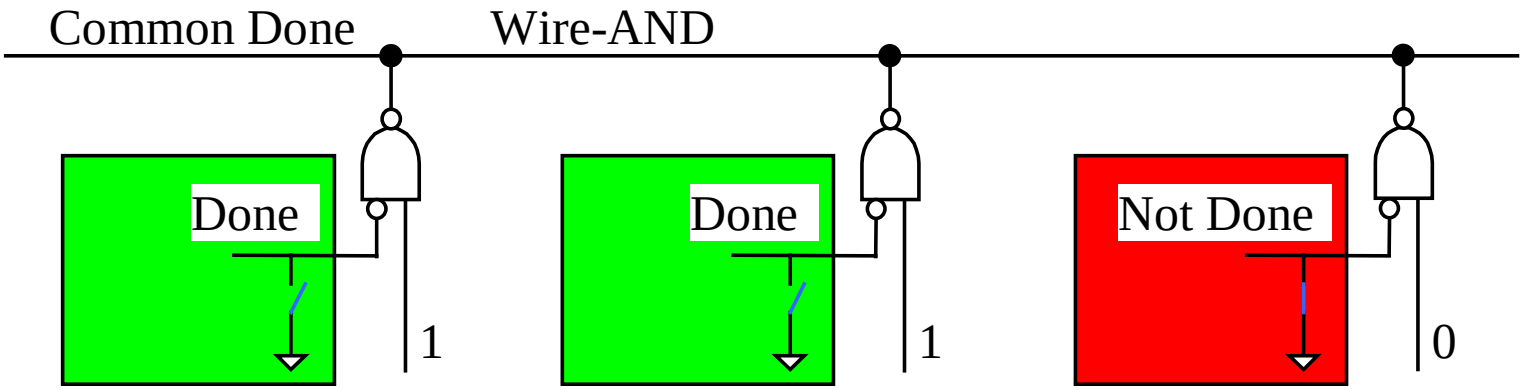
R. Staley

THE UNIVERSITY OF BIRMINGHAM

… which causes the configured FPGAs to 'sleep' until ALL FPGAs in the group have been configured. … fault tolerance , development?

Luckily , this default behaviour can be over-ridden, and the FPGAs can be made to 'wake-up' before DONE is released.
(Keywords - BitGen , GTS , GSR and GWE).

Next revision of CPM design will condition the DONE signals:



R. Staley

THE UNIVERSITY
OF BIRMINGHAM

Mechanical Items

Mechanical Stability.

Unresolved.

Guide Rails.

Longer rails have arrived but …

R. Staley

THE UNIVERSITY OF BIRMINGHAM

Next

Serialiser in Playback mode to Generate 160Mb/s data.
Requires TTCRx Controller to be working

Configure a single CP FPGA.

Configure all CP FPGAs

Configure ROC and Hit FPGAs

Obtain TTCDEC card and test TTCRx Interface

…

R. Staley

THE UNIVERSITY
OF BIRMINGHAM

Summary

Making steady progress with development.

- Reliable access to FLASH memory
- FPGA configures from FLASH memory

Very difficult to probe module inside crate