DSS Firmware Updates

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RAL

Introduction

- Contents of PCO 001.
- Designs affected.
- Problems * / Solutions.
  - * Also known as "*Design Features*".
- Design Verification in R25 HDL.
- Future Modifications.

Project Change Order - 001

- This was finally signed off on 9th May 2002 and work commenced.

Item 1

- Use dual-port memory (DPRAM) as a test source for testing other variants of ROD firmware.
- This requires a programmable register to control the length of the DAV signal.

Item 2

- DPRAM read/ write 32 bit words and automatic comparison test of 32 bit words to use with the general purpose I/O CMC (GIO).

Item 3

- 32K wraparound on the DPRAMs to be changed to a programmable depth. The DSS will require two programmable comparators "short_mem" (16 bit) and "long_mem" (16 bit) to determine the memory addresses at which wraparound to zero occurs, plus a programmable "orbit" register and an orbit_countdown counter (32 bit).

Item 3 continued...

- a.
  - On reset (on power-up and "Address Counter Reset"), "orbit" is copied to "orbit_countdown" and mem_address is set to 0.

Item 3 continued...

- b.
  - The memory address is incremented each 25 ns. The DSS now plays the memory contents through the GIO daughter board.

Item 3 continued...

- c.
  - When memory_address reaches short_mem AND orbit_countdown is non zero, mem_address is reset to 0. If the front panel BUSY input is present, orbit_countdown is decremented by 1 (This is the end of a single orbit data set).

Item 3 continued...

- d.
  - When memory_address equals long_mem, mem_address is reset to 0 and orbit_countdown is reloaded from "orbit". (This is the end of a multiple-orbit data set)

Designs to Modify

- Item 1
  - Change for "ROD Test Source".
- Items 2 and 3
  - Modification for the GIO daughter card.
    - This is basically the LVDS cards design of old.
  - Required changes to both the Transmitter (Item 3) and Receiver (Item 2).

Additional Modification 1

- The Xilinx CPLD on the DSS required modification in order to cope with the increased number of registers.
  - Created decoding for an extra 2 registers in each Data FPGA.
  - Also added the capability of an additional 2 registers in the SLINK FPGA's.

Additional Modification 2

- The routing of the “BUSY” signal to the DATA FPGA’s was required.
  - This signal is an input to the Altera CPLD only. The use of sending this signal out on a *spare* pin was prohibited as all spare capability between the Altera CPLD and the DATA FPGA’s was already being used.
- SERIOUSLY BAD NEWS... THINK AGAIN

The Fix

- Devised a scheme where the “BUSY” signal was encoded onto a pre-existing net. Used the “start” net.
  - Start pulsing LOW for 25 ns signals the system is BUSY.
  - Start pulsing LOW for 50 ns signals that the system is NOT BUSY.

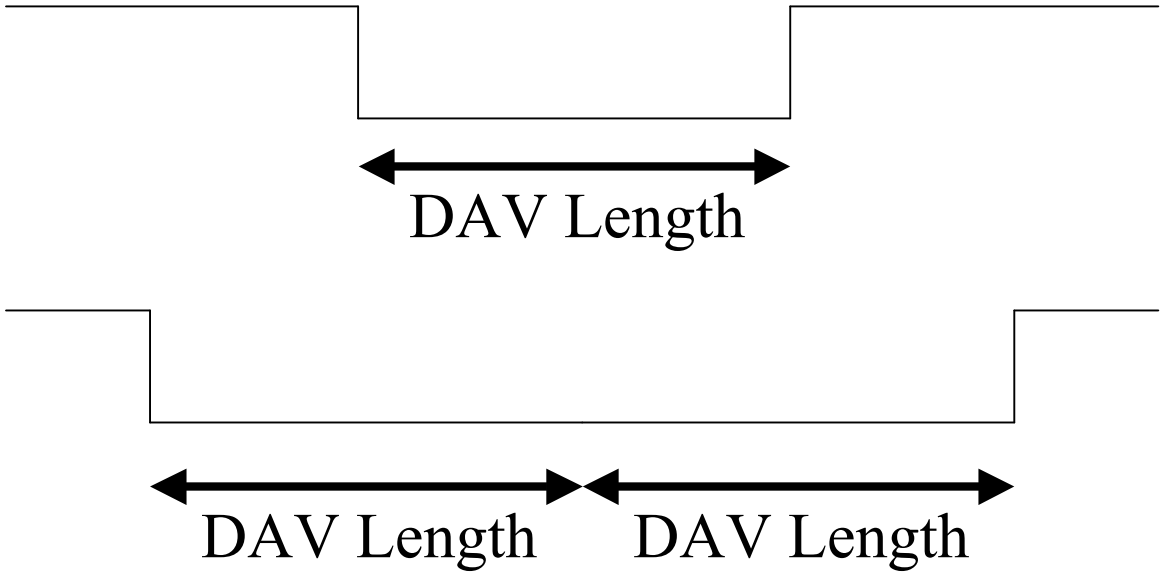
Update DSS CPLD's

- So far only DSS's with serial numbers 01 and 03 have been updated CPLD's.
- Others MUST be updated before using with latest firmware.

ROD Test firmware

- The "ROD Test" firmware now has a new version/type code of 0216 hex.
  - DAV length register is at the following addresses:-
    - Daughter Card 1:-
      - 108,10C, 110 and 114. (hex)
    - Daughter Card 2:-
      - 118,11C, 120 and 124. (hex)
- The DAV length register (8 bit) powers up to 84 decimal. i.e. Slice Data.

Variable DAV Length



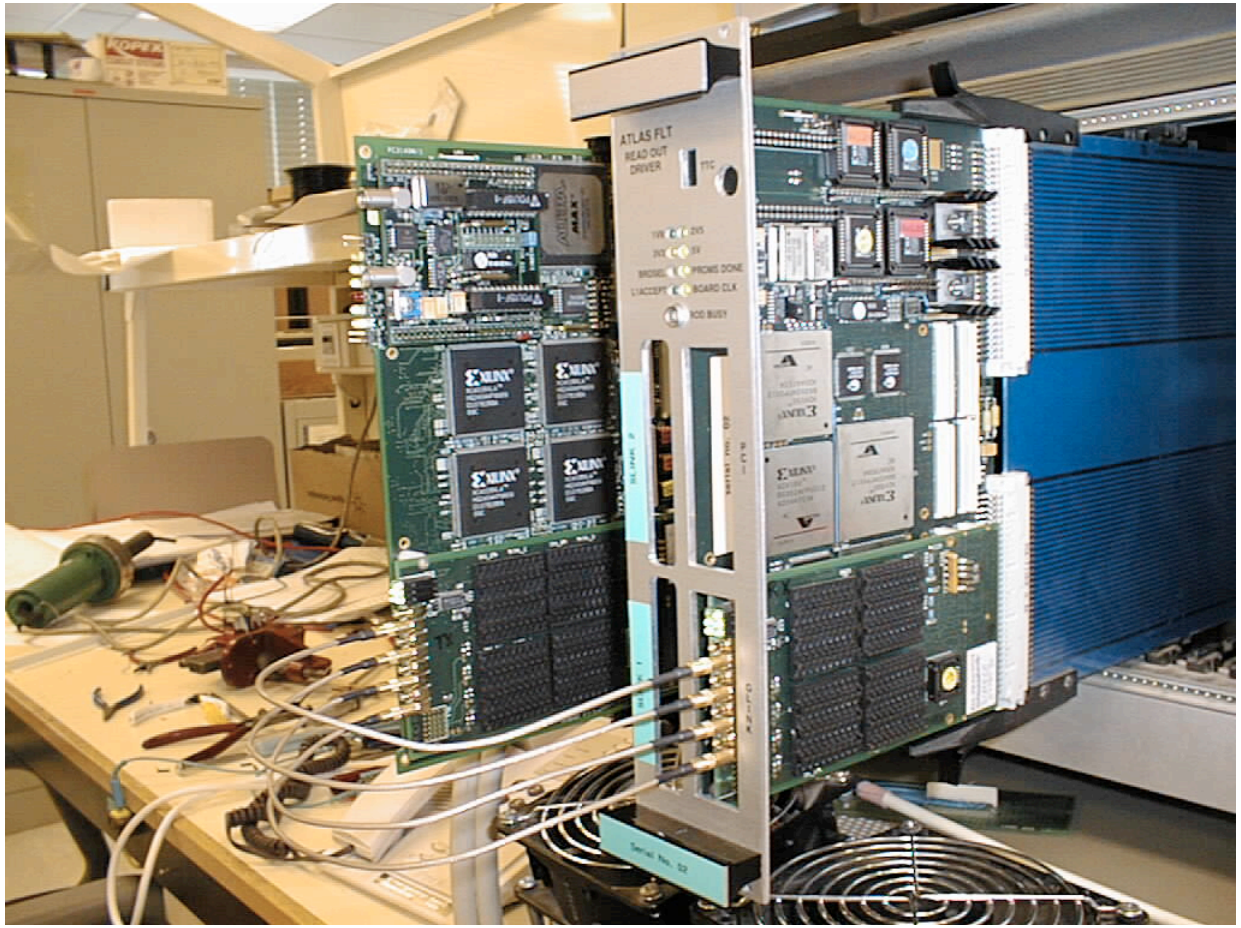
Single slice or ROI

Multiple slice operation i.e. 2 slices

Design Verification

- Performed limited tests in R25 HDL using DSS and ROD with the Glink Tx and Rx cards.
  - Results indicated that basic data transfer was still working.
  - Release firmware to Bruce on 28th May 2002 for extensive tests.
    - At time of writing have not received any complaints.

ROD Test Setup



GIO daughter card - New versions

- The new LVDS Source for GIO has version/type code of “0612” hex.
- The new LVDS Sink for GIO has version/type code of “0A13” hex.

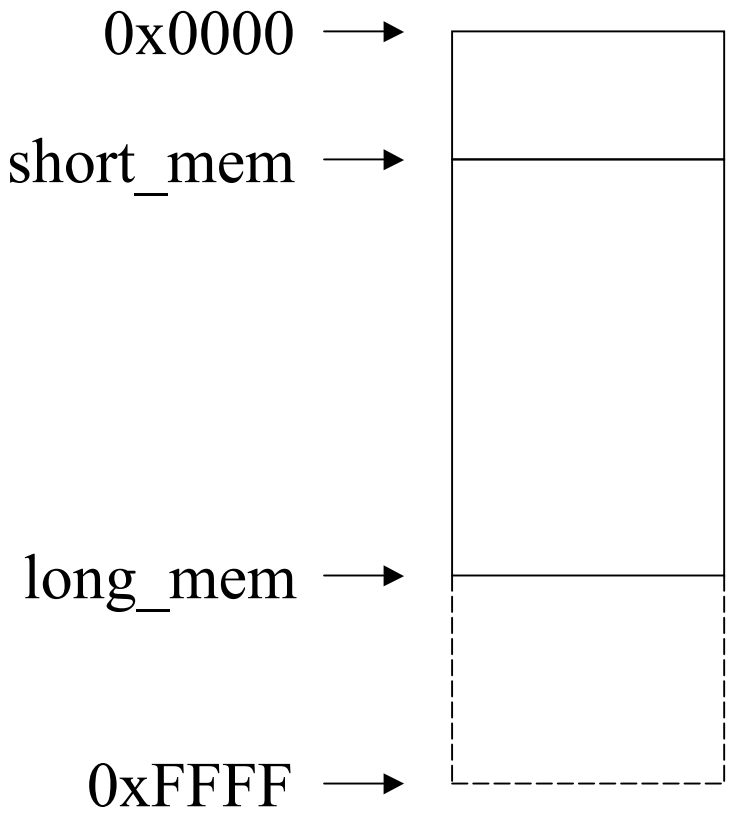
GIO daughter card - Source 1

- Orbit register (32 bits) is at:-
  - Daughter Card 1:-
    - 108,10C, 110 and 114. (hex)
  - Daughter Card 2:-
    - 118,11C, 120 and 124. (hex)
- Note
  - This occupies the same address space as DAV register in "ROD test" design.

GIO daughter card - Source 2

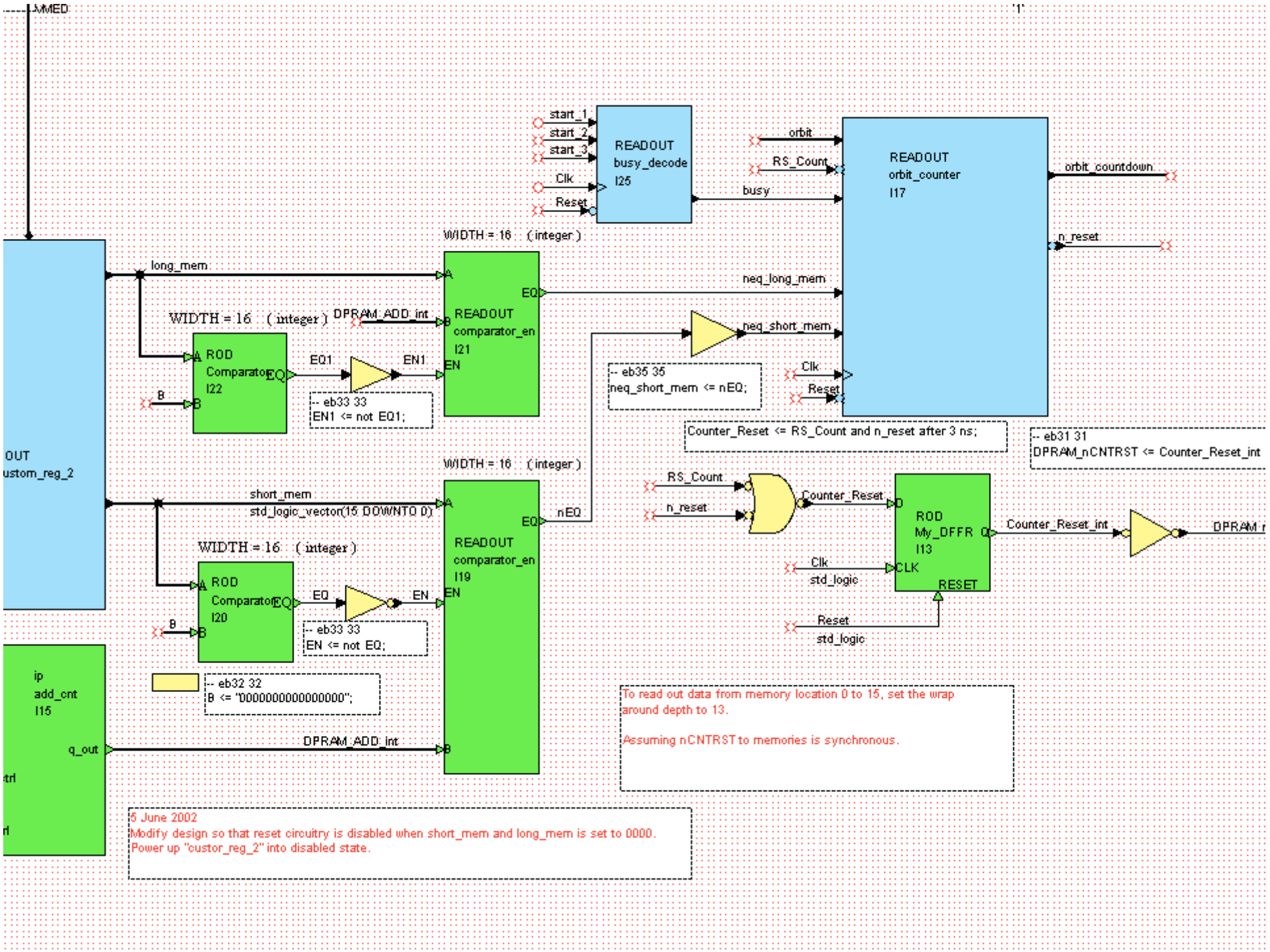
- Long mem / Short mem
  - bits 31 - 16 / bits 15 - 0
- Registers at addresses:-
  - Daughter Card 1:-
    - 130,134, 138 and 13C. (hex)
  - Daughter Card 2:-
    - 140,144, 148 and 14C. (hex)

Memory Diagram



if orbit_countdown in not zero then
reset memory pointer to zero
if BUSY then
dec orbit_countdown

reset memory pointer to zero
reload orbit_countdown from register


start_1
start_2
start_3
Clk
Reset
READOUT
busy_decode
I25
busy
orbit
RS_Count
READOUT
orbit_counter
I17
orbit_countdown
n_reset
WIDTH = 16 (integer)
long_mem
READOUT
comparator_en
I21
EQ
neq_long_mem
DPRAM_ADD_int
ROD
Comparator
I22
EQ1
EN1
B
-- eb33 33
EN1 <= not EQ1;
neq_short_mem
-- eb35 35
neq_short_mem <= nEQ;
Clk
Reset
Counter_Reset <= RS_Count and n_reset after 3 ns;
-- eb31 31
DPRAM_nCNTRST <= Counter_Reset_int
WIDTH = 16 (integer)
short_mem
std_logic_vector(15 DOWNTO 0)
nEQ
RS_Count
n_reset
Counter_Reset
ROD
My_DFFR
I13
Counter_Reset_int
Clk
std_logic
RESET
Reset
std_logic
WIDTH = 16 (integer)
ROD
Comparator
I20
EQ
EN
-- eb33 33
EN <= not EQ;
-- eb32 32
B <= "0000000000000000";
ip
add_cnt
I15
q_out
DPRAM_ADD_int
To read out data from memory location 0 to 15, set the wrap around depth to 13.
Assuming nCNTRST to memories is synchronous.
5 June 2002
Modify design so that reset circuitry is disabled when short_mem and long_mem is set to 0000.
Power up "custor_reg_2" into disabled state.

Possible Problems / Design Features

- The design relies upon the counter in the FPGA keeping track with the address counter in the memory chips.
- Due to latency in the design short_mem and long_mem should be set to a value of 2 less than the last data memory location required.

Design Features Continued...

- Setting both long_mem and short_mem to 0x0000 will disable the RESET mechanism and allow rollover at 32k as normal.
- After loading the orbit_countdown register you should apply an “Address Counter Reset” to ensure that the value is transferred to the orbit_countdown counter.

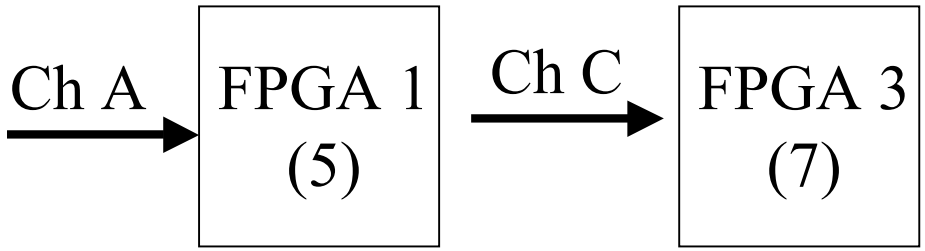
GIO daughter card - Sink 1

- Compare Mask (20 bits)
  - Daughter Card 1:-
    - 108,10C, 110 and 114. (hex)
  - Daughter Card 2:-
    - 118,11C, 120 and 124. (hex)

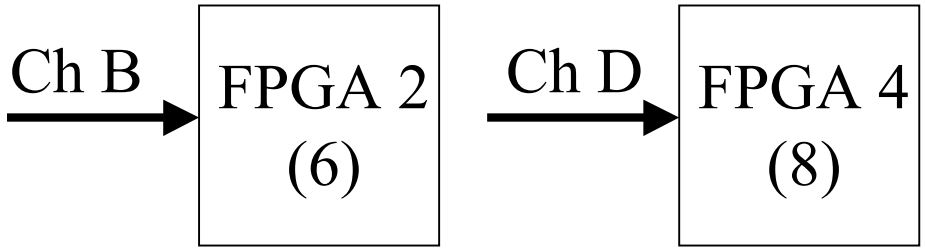
GIO Daughter Card - Sink 2

- Set bit high to disable the comparison of that data bit.
  - This allows the GIO data width of 32 bits to run within a design that originally allowed a data with of 80 bits (Previous daughter cards such as Glink or LVDS has data widths of 4x20).
    - FPGA 1 (5) - 20 bits
    - FPGA 2 (6) - 12 bits
      - () indicate Daughter card in slot 2.

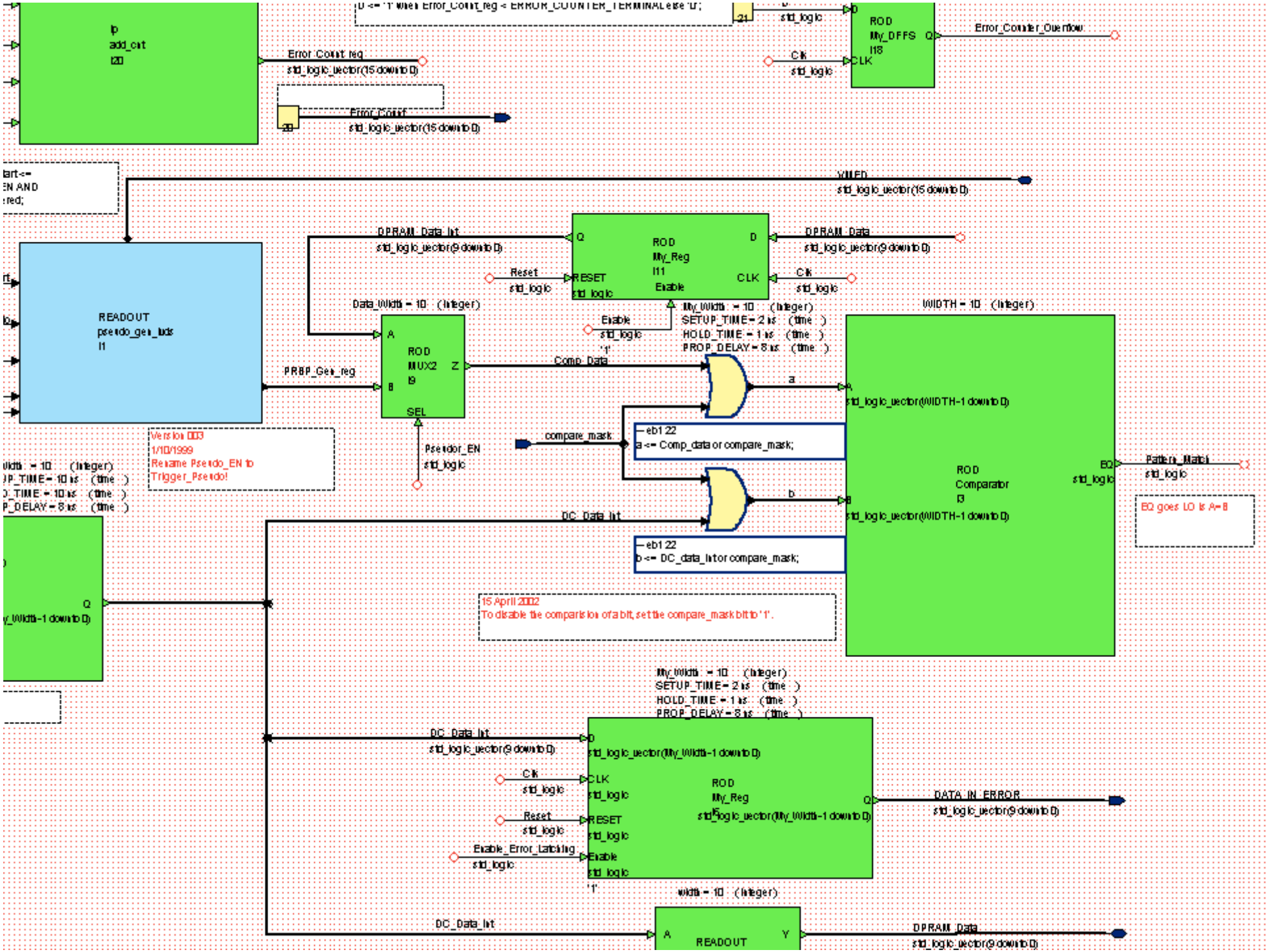
Automatic Comparison



Glink Cards
A, B, C and D
are 20 bits.



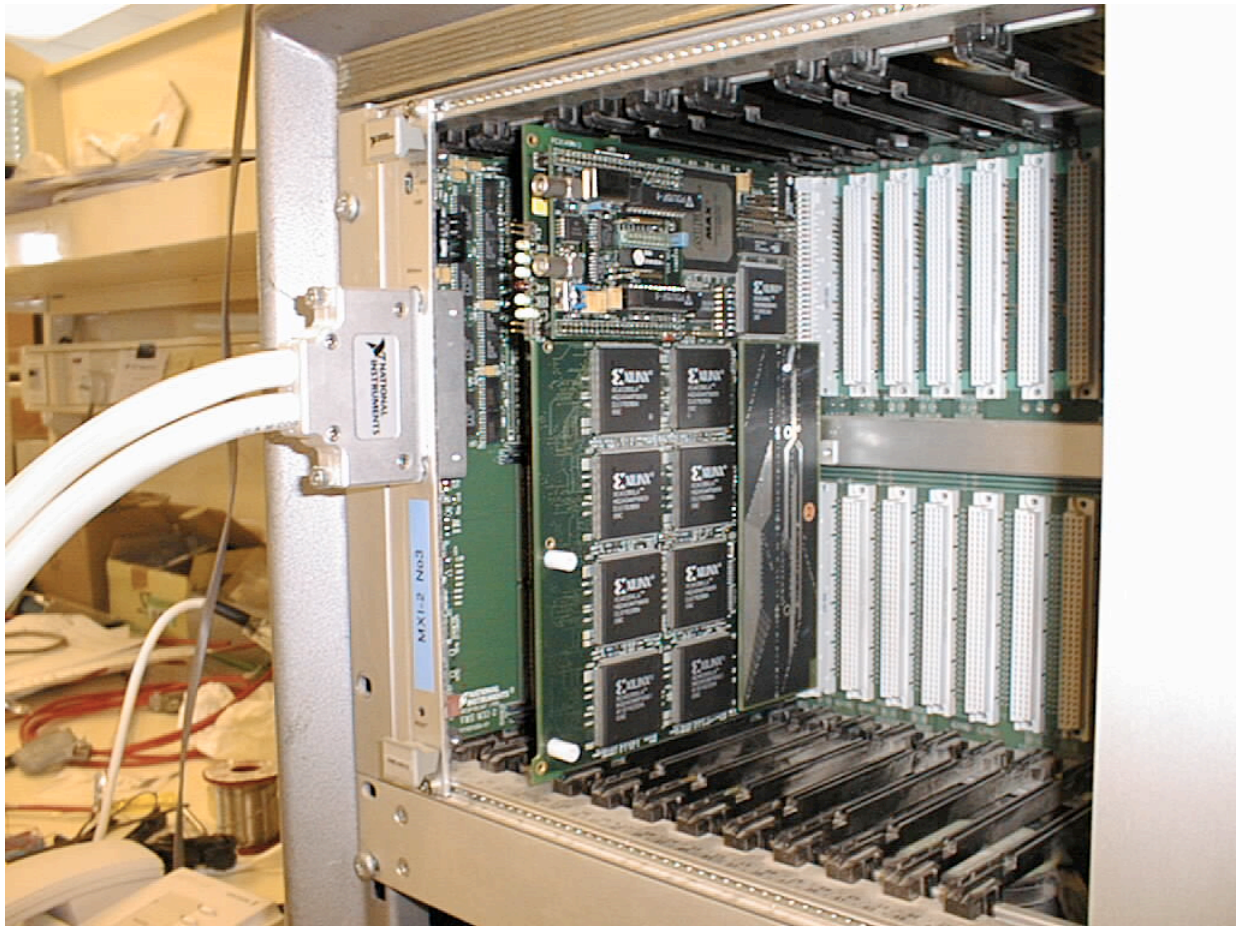
GIO Card
A - 20 bits
B - 12 bits


lp
add_cst
I20
Error_Count_reg
std_logic_vector(15 downto 0)
Error_Count
std_logic_vector(15 downto 0)
ROD
My_DFFS
I18
Clk
std_logic
Error_Counter_Overflow
VALID
std_logic_vector(15 downto 0)
READOUT
pseudo_gen_tds
I1
DPRAM_Data_Int
std_logic_vector(9 downto 0)
ROD
My_Reg
I11
Enable
Reset
std_logic
DPRAM_Data
std_logic_vector(9 downto 0)
Data_Width = 10 (integer)
ROD
MUX2
I9
PRBP_Gen_reg
Comp_Data
Pseudo_EN
std_logic
Version 003
1/10/1999
Rename Pseudo_EN to
Trigger_Pseudo!
compare_mask
eb1 22
a <= Comp_data or compare_mask;
b <= DC_data_Int or compare_mask;
DC_Data_Int
My_Width = 10 (integer)
SETUP_TIME = 2 ns (time)
HOLD_TIME = 1 ns (time)
PROP_DELAY = 8 ns (time)
WIDTH = 10 (integer)
ROD
Comparator
I3
EQ
Pattern_Match
EQ goes LO is A=B
15 April 2002
To disable the comparision of a bit, set the compare_mask bit to '1'.
Enable_Error_Latching
DATA_IN_ERROR
width = 10 (integer)

Design Verification

- Performed limited tests in R25 HDL using RAMP data and LOOPBACK card.
  - Results seemed to indicate that the RESET mechanism was working as expected.
  - Firmware ready for release for extensive tests in R1 on 27th May 2002.

GIO Test Setup



Firmware on WWW

Device Firmware	Current Version	Modification Date	Comments
VME Decoder	6	28/05/2002	
VME Registers	16	28/05/2002	Add additional register decoding.
LVDS Source	6	28/05/2002	Pseudo Ramp Source
LVDS Sink	10	28/05/2002	Pseudo Ramp Sink
G-Link Source	10	7/12/2000	
G-Link Destination	11	10/8/2000	
S-Link Source	5		
S-Link Destination	6	23/10/2000	
ROD Test	2	28/05/2002	Use with Glink Tx card

http://www.te.rl.ac.uk/local/ESDG/SDG/Projects/atlas-flt/external/firmware%20folder/dss/firmware.html

Additional Requests 1

- It has been suggested that these additional registers cause problems with the diagnostic software as different cards have different register space, requiring a different module definition file for each combination of daughter cards.
- “Solution” is to add extra un-used registers.

Additional Requests 2

- If required, additional r/w registers can be added.
  - This could affect up to 6 designs so is not a trivial task.
- Don't mention the 6 1/2 hours required to add a divide by 2 circuit to the 40 MHz clock to the CP chip for Richard.

Compromise

- Have agreed to add “dummy” registers to all future DSS Data FPGA designs.
- This modification will not be released until I am required to change a design for “technical” reasons.

Acknowlegements

Summary

- 5 designs modified in total.
- Basic tests in R25 HDL indicate that PCO 001 has been completed.
- Require further extensive testing in R1.