The Common Merger Module: Status Report

- Hardware
- **CMMs:**
- 5 boards manufactured
- 2 sent for assembly, expected back next week.

- **RTMs:**
- Panagiotis has finished schematic entry and layout.
- Waiting to get our hands on backplane before we decide on mechanics & dimensions of board.

- **DSS LVDS drivers/receivers:**
- In drawing office.

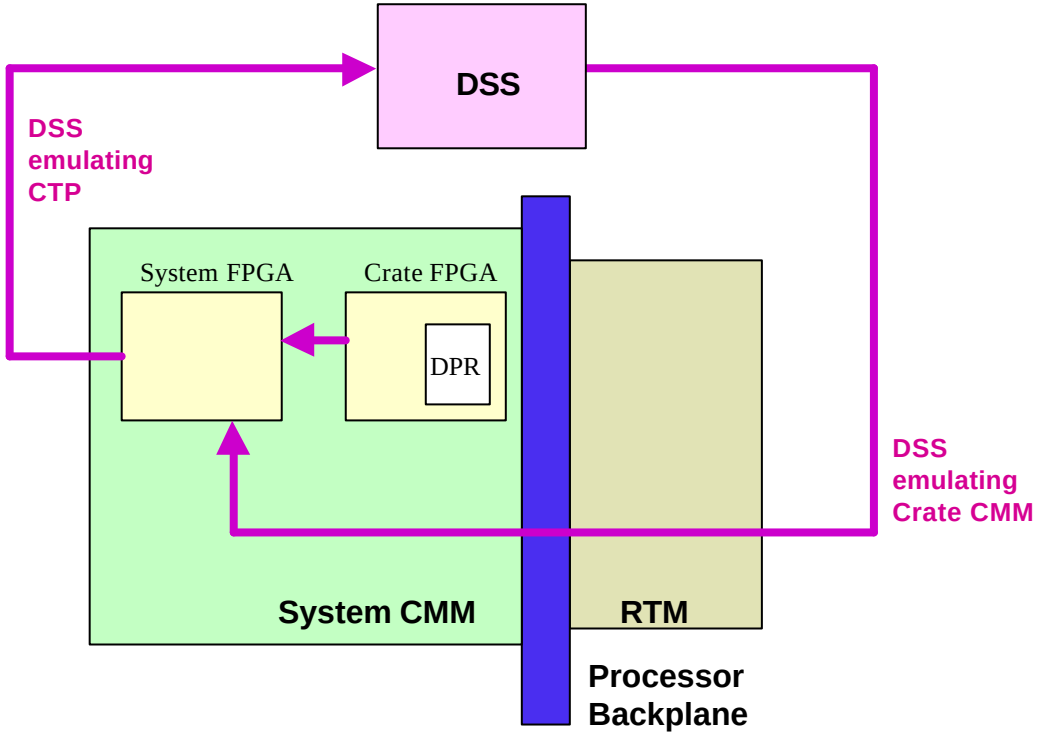
- **Firmware**
- Crate FPGA:Crate & Sys versions ✓
- System FPGA:Crate & Sys versions ✓
- VME controller (CPLD) ✓

- I2C controller: pending
- Flash Memory controller: pending

- Pending items:
  - Waiting for Richard to, very kindly, supply us with code.
  - Initial testing not held up by absence of this code.
  - VME-loading of Flash memories can be bypassed by use of socketed devices.

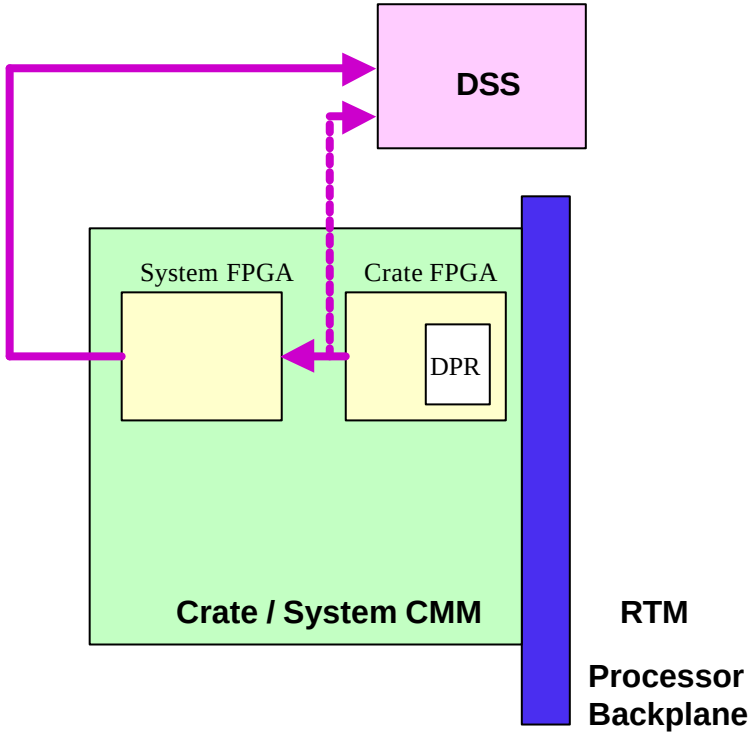
Initial Test Plan (1)

- **Aim of *initial* tests*:* reach situation where we can do this:**



Initial Test Plan (2)

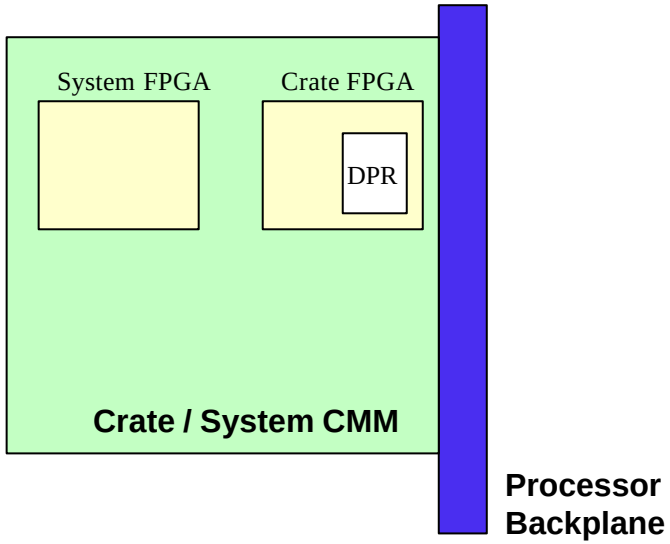
- **But before this, with no RTM available:**



- Use DPR as data source
- Can perform initial tests of Crate and System level merging logic.

Initial Test Plan (3)

- **But before this…**



- **With no DSS:**
- Can't do anything with real-time data path, but plenty of other things to test:
- Configuration mechanism
- VME interface
- Flash memory loading via VME
- I2C controller
- CAN bus
- Plenty for us to do if no hardware other than crate available.

- **With no Crate:**
- dead duck