Ideas for CMM Test Procedures

- **Six stages of testing:**

1.	Module "health checks" *(mechanical, power, etc)*	*(STANDALONE)*
2.	Bench tests (*JTAG, VME--, FPGA configuration, CAN, ...)*	*(STANDALONE)*
3.	Read-out of pre-loaded Slice data into ROD	*(+ROD)*
4.	Real-time emulated data-flow operation *(Crate level)*	*(+CPME2/DSS+ROD)*
5.	Real-time emulated data-flow operation *(System level)*	*(+CMM+CPME2/DSS+ROD)*
6.	Real-time true data-flow operation *(System level)*	*(+CMM+CPMs(2)+ROD)*

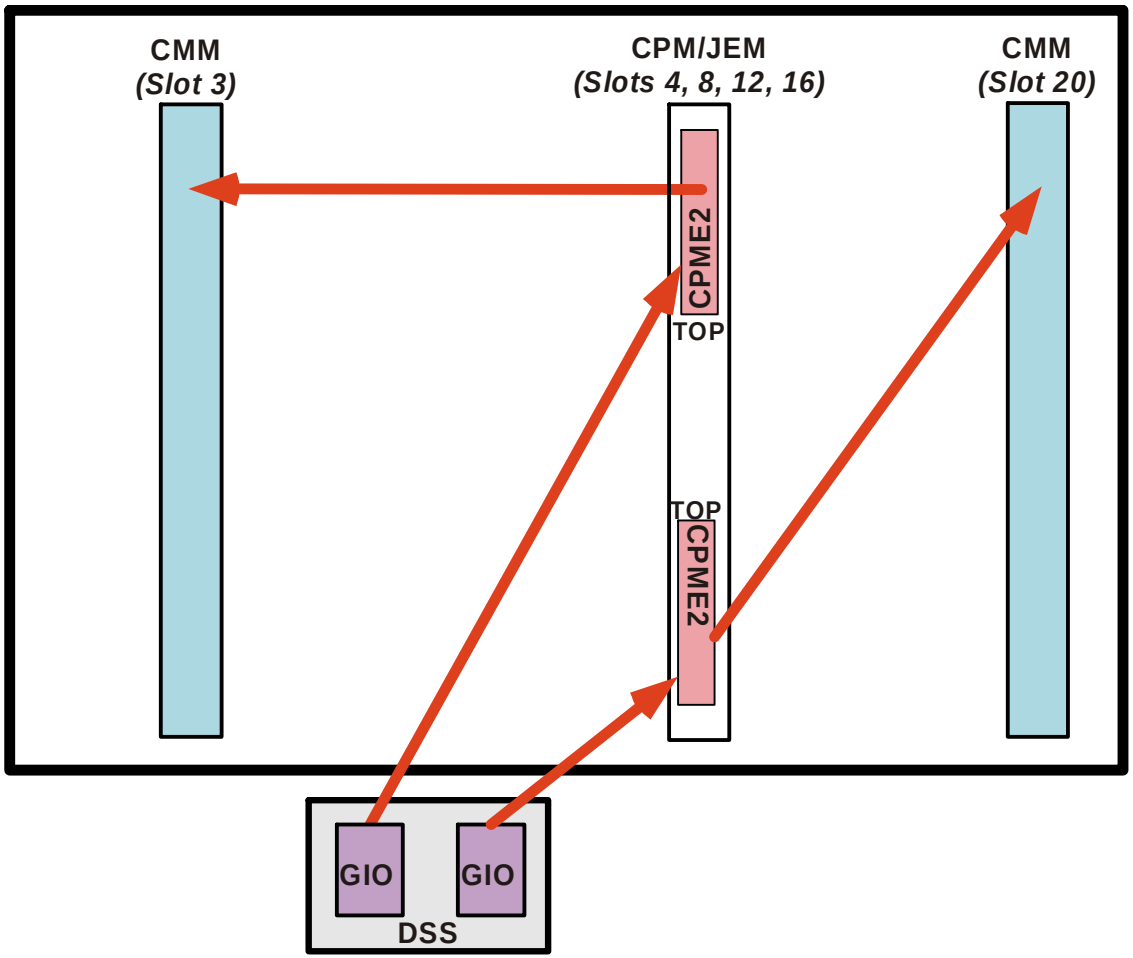
- **Lots of hardware + firmware + software needed almost from Day 1**
- **First two stages are in Electronics Test Lab *(I Brawn, R Matson, A Davis)***
  - **9U Crate/Backplane + PSU + Cooling Fan Tray needed immediately *(w/b 4 March)***
- **The final part of Stage 2 testing should check all registers and scrolling data memories for correct R/W operation**

Ideas for CMM Test Procedures

- **Final four stages are in Lab 12 *(PPD Group + engineer help when needed!)***
- **Stage 3 - Read-out of pre-loaded Slice data into ROD**
  - ***Requires TCM, TTCdec, D-ROD***
  - **Set up TTC system - TCM + TTCdec on CMM**
  - **Load test data pattern - e.g. ramp - into scrolling input memories via VME, channel by channel**
  - **In Playback mode, propagate these data patterns through the merging algorithms into scrolling output memory**
  - **Stop clocks and read output memory via VME**
  - **Repeat tests with L1A transferring Slice data into D-ROD at up to 100KHz *(needs appropriate firmware)***
  - **Explore timing margins**

Ideas for CMM Test Procedures

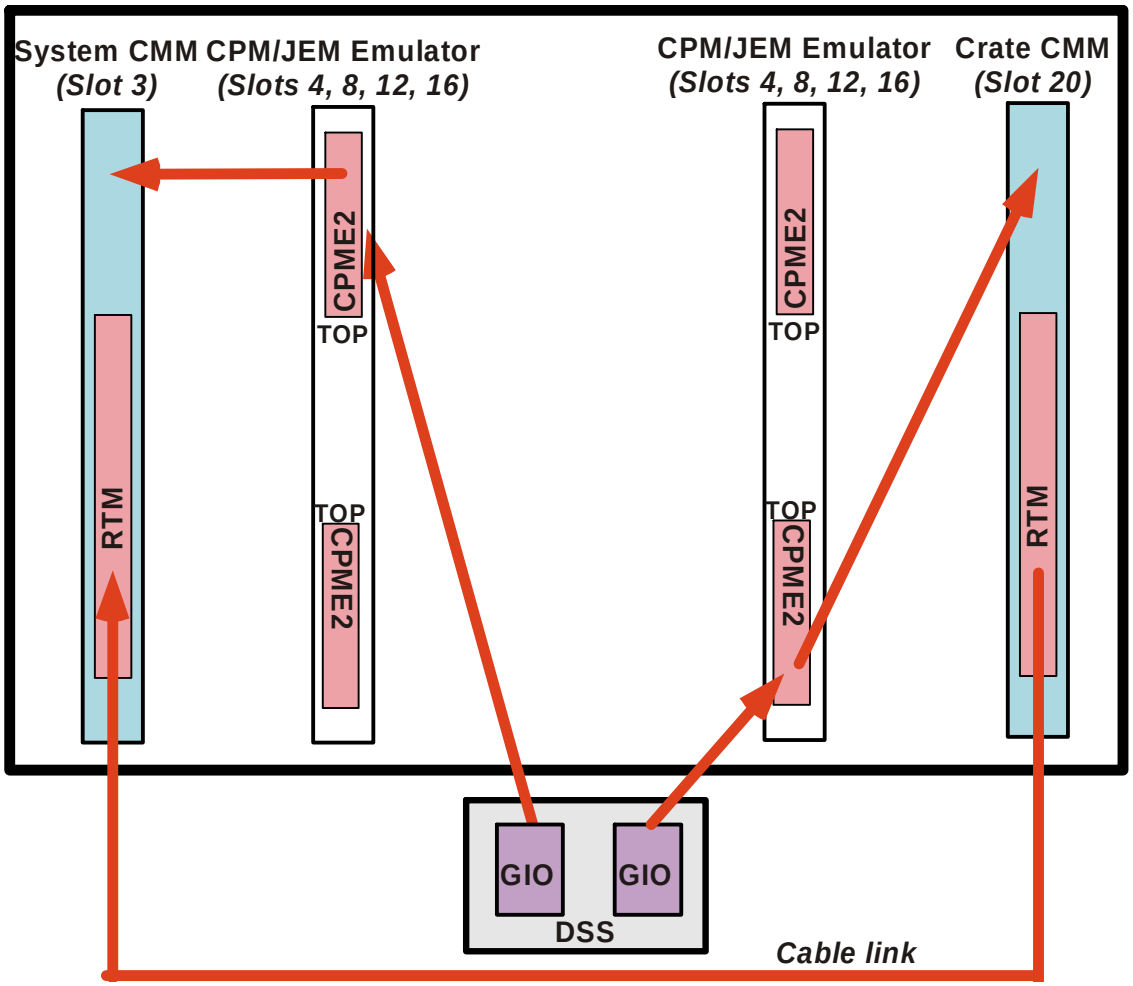
- **Stage 4 - Real-time emulated data-flow operation *(Crate level)***



- ***Requires CMM, TCM, TTCdec, D-ROD, CPME2 (2), DSS, GIO (2)***
- **Load DSS with data patterns *(ramps, etc)***
- **With CPME2 in each of 4 possible CPM slots, clock data into CMM via PB**
- **Stop clocks, read input memories via VME, check correct data capture**
- **Tune timing as needed**
- **Repeat with L1A triggers at up to 100KHz and read out ROD data**
- **Verify correct algorithm performance**

Ideas for CMM Test Procedures

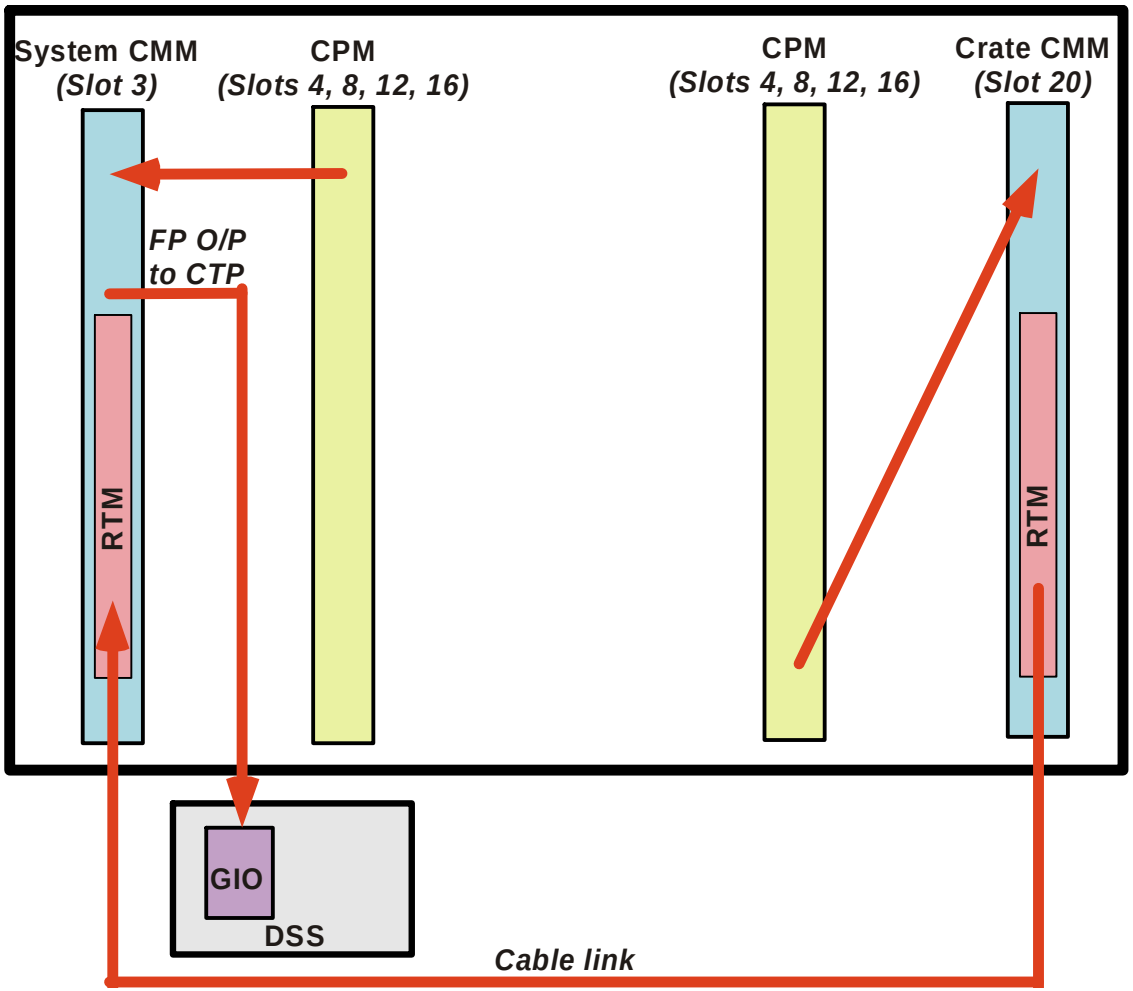
Stage 5 - Real-time emulated data-flow operation *(System level)*



- *Requires CMM (2), TCM, TTCdec (2), D-ROD, CPME2 (2), DSS, GIO (2), RTM (2)*
- Load DSS with data patterns *(ramps, etc)*
- With CPME2s in a pair of the 4 possible CPM slots, clock data into Crate CMM and System CMM via PB
- Stop clocks, read System CMM input memories via VME, check correct data capture
- Adjust System CMM pipeline delay as needed to merge data correctly
- Repeat with L1A triggers at up to 100KHz and read out D-ROD data
- Verify correct algorithm performance

Ideas for CMM Test Procedures

Stage 6 - Real-time true data-flow operation *(System level)*



- *Requires CMM (2),TCM, TTCdec, D-ROD, DSS, GIO, RTM (2), CPM (2)*
- Load CPMs with data patterns *(ramps, etc)*
- With CPMs in a pair of the 4 possible CPM slots, clock data into Crate CMM and System CMM via PB
- Stop clocks, read Crate and System CMM input memories via VME, check correct data capture
- Read out DSS and verify correct CTP data
- Repeat with L1A triggers at up to 100KHz and read out D-ROD data
- Verify correct algorithm performance