CP chip tests and simulation model

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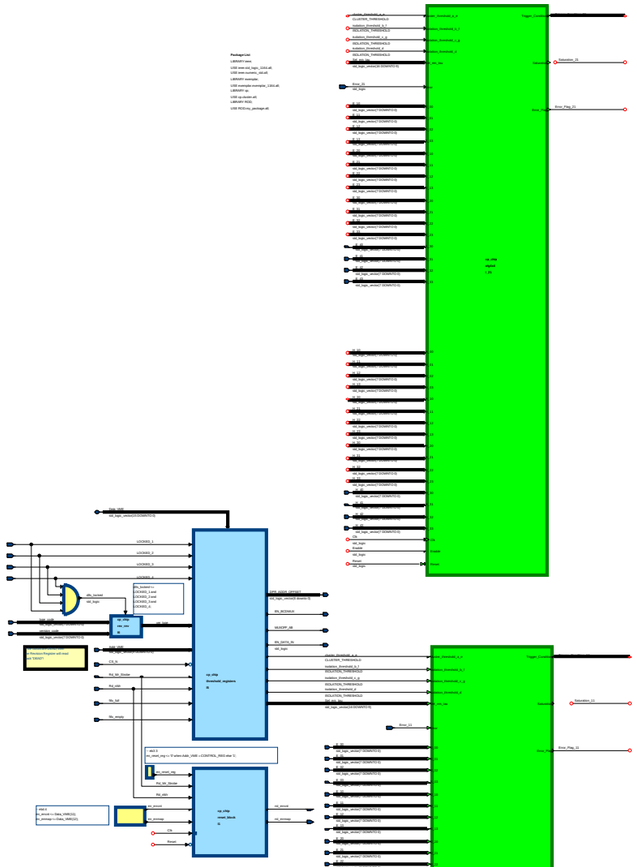
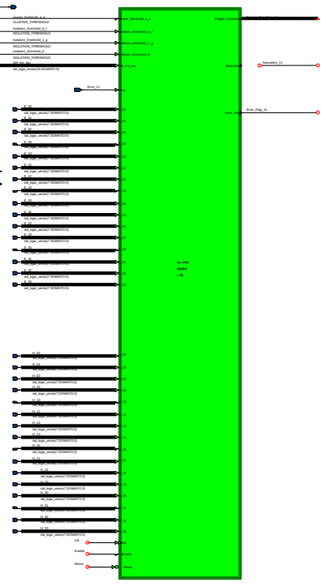
CP chip tests

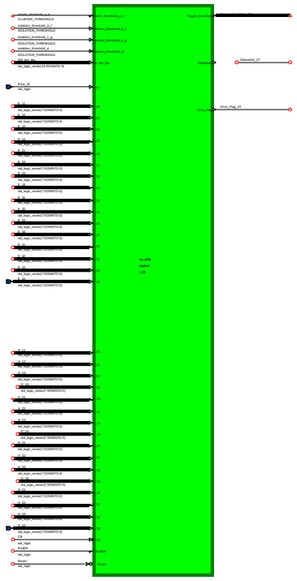
- Unable to proceed any further
  - Gone as far as I can with my limited GTM test set-up.
  - Awaiting “real” hardware - IMMINENT?

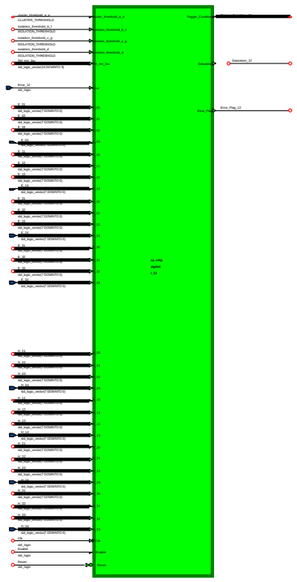
CP simulation model

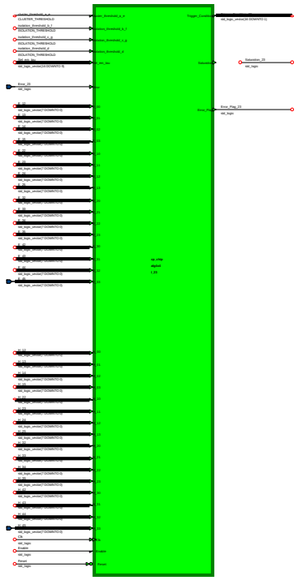
- Investigated this in some detail
  - Found a way to compile the design into a stand alone library for simulation with modelsim.
  - Internal signals are fully accessible.
  - Source code is protected.
  - Can supply some diagrams of structure.
  - A reasonable compromise.

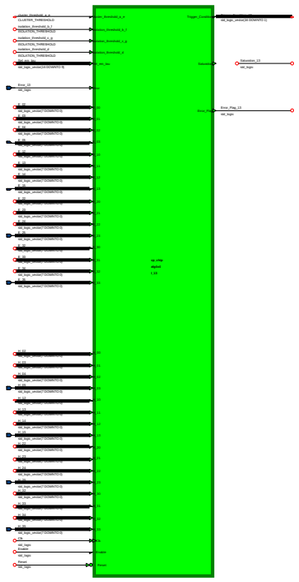


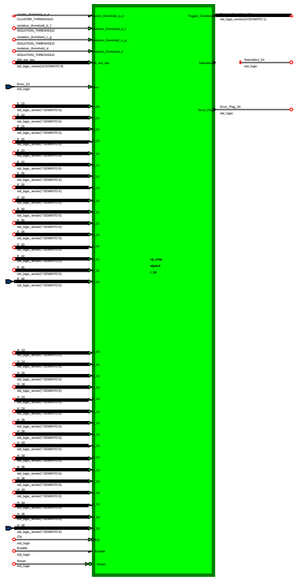


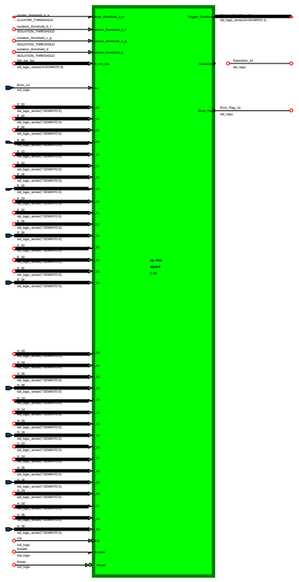


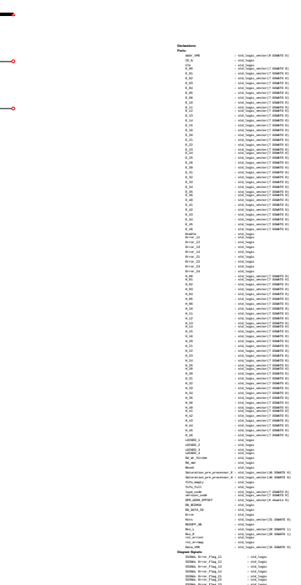


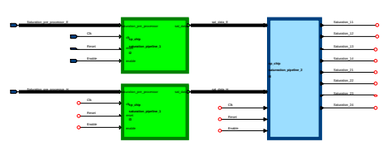


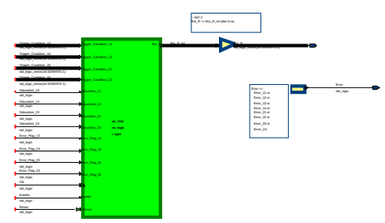






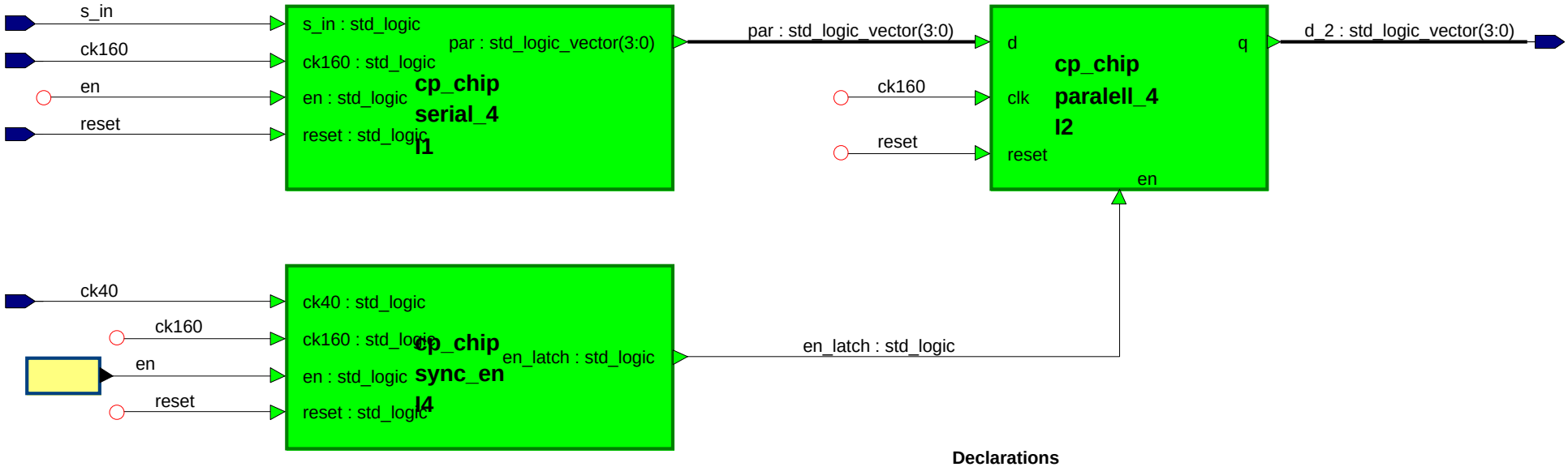






Package List

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all;
```




```
-- eb1 1
en <= '1';
```

Declarations

Ports:

```
    ck160     : std_logic
    ck40      : std_logic
    reset     : std_logic
    s_in      : std_logic
    d_2       : std_logic_vector(3 DOWNTO 0)
```

Diagram Signals:

```
    SIGNAL en       : std_logic
    SIGNAL en_latch : std_logic
    SIGNAL par      : std_logic_vector(3 DOWNTO 0)
```