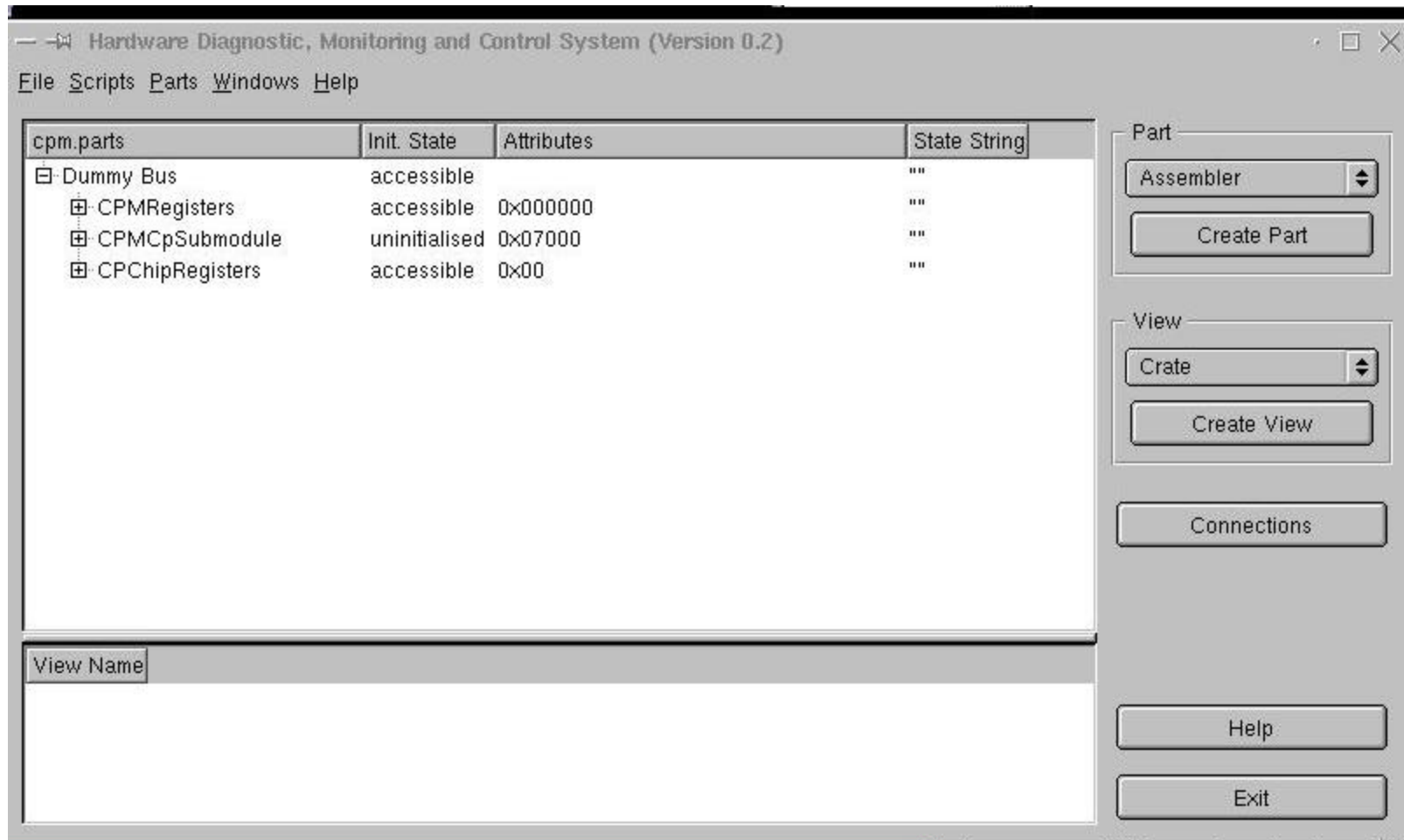


# Cluster Processor Module Status

# S/W Status

- HDMC part file nearly ready for the CPM: need serialiser part
- Use SubModule structure for CpChip and SrlChip.
- Submodule for ROC? Hit?...not really necessary
- Register classes automatically generated with Regbuild: useful for Module Services

# HDMC panel for 1 CPM



# HDMC Panel SubModule

List of  
CP chips {

Register  
of CP  
chips {

Hardware Diagnostic, Monitoring and Control System (Version 0.2)

File Scripts Parts Windows Help

cpm.parts	Init. State	Attributes	State String
[-] Dummy Bus	accessible		""
[-] CPMRegisters	accessible	0x000000	""
[-] CPM CpSubmodule	uninitialised	0x07000	""
[-] Chip[0:0]<0>	uninitialised	0x7000	""
[-] Chip[0:1]<1>	uninitialised	0x7800	""
[-] Chip[0:2]<2>	uninitialised	0x8000	""
[-] Chip[0:3]<3>	uninitialised	0x8800	""
[-] Chip[0:4]<4>	uninitialised	0x9000	""
[-] Chip[0:5]<5>	uninitialised	0x9800	""
[-] Chip[0:6]<6>	uninitialised	0xA000	""
[-] Chip[0:7]<7>	uninitialised	0xA800	""
[-] <b>CPChipRegisters</b>	accessible	0x00	""
CpFwVR	accessible	0x0; CPM.CpFwVR; Read/Write	""
CpFwCR	accessible	0x01; CPM.CpFwCR; Read/Write	""
CpFwSR	accessible	0x2; CPM.CpFwSR; Read/Write	""

Part: Assembler [v] Create Part

View: Crate [v] Create View

Connections

Help

Exit

# F/W Status

- F/W need further work such as implemented F/W version...any rule?
- CP F/W code received: too big for our local PC...but manage to do some work
- Meanwhile, receive new PC faster and bigger RAM (800 MB)...but license problem. Flexlm (license manager) detect wrong host ID. Paul Hardy has been contacted.

# VHDL simulation of CP algorithm

- Build a test bench:
  - to read F/W version and Control Register
  - generate calibration pattern for the timing calibration: 1010010110100101...
- ...does not seem to give any satisfying results in both cases
- Need double check test bench with James
- Resolution used was ns , James ps
- Need to be tested with new PC...
- Future: why not thinking adding other F/Ws and simulate Srl + Cp + RoC + Hit + VME

# H/W testing of CP algorithm of one CP chip

- Idea: plug a card near CPM under test and re-direct BP signals from others CP chips to provide missing signals to the CP chip tested.
- Problems: we need to access all the CP chips of the card to have all the signal required: timing is a problem
- Even tested half of the CP algorithm, 2x4 TT, required to populate nearly 3/4 of the PB
- A board will be build to at least read and check signals fanned out from a BP connector