

Heidelberg Status



- PPr ASIC being fabricated 3 wafers will be fully-processed, 3 partially to allow for mask updates at later stage - completion ~end-March
- PPr MCM also being fabricated at Wurth 100 substrates ~mid-March
 - Final assembly (passive components, die-attachment, etc) will be done at KIP
 - Test card still being designed
- PPM schematics mostly done some remaining areas
 - LVDS fan-out implementation LFANs or Xilinx device (would first need bench tests)
 - ReM FPGA (*D Kaiser*) design continues PPM layout awaits final pin-allocation
 - Another CAN processor (Lawicel) Atmel **nc**ontroller, small (DIL28), needs external ADC
- **TCM** arrived in KIP its matching ALC now being designed
- No further news on PPr ROD

◆ 160 LVDS cables available (4 channels, 15m length) - each CPM needs 20



Mainz Status



- JEM-0 #1 testing continues
 - VME access to FPGAs currently being worked on real-time data paths exercised "soon"
- JEM-0 #2 also now assembled
 - Assembly and re-work problems now seem solved with new (expensive) company
 - Powered up successfully JTAG testing starting ~now
- Two more JEM-0s needed for Slice Tests
- JEM0 uses TileCal TTCrx d-card not enough for 4 JEM-0s
 - Use TTCdec? Needs yet another Interposer card to adapt it
- Improved Jet algorithm (work by Stockholm students)
 - Latency reduced by 0.5 ticks (VHDL simulation) will be incorporated into JEM-0 modules
- ◆ JEM-0 still to be brought into HDMC framework



Stockholm Status



- Backplane manufacture complete delivery to Stockholm 22 February
 - Temporary glitch missing power pins shipping separately ~now
- First Crate/Backplane should be at RAL during w/b 4 March
- PSU needs to be connected to Crate/Backplane, and complete system tested before JTAG tests on first CMM and CPM
- Second Crate/Backplane will be sent to RAL for w/b 11 March, then transferred to Birmingham with its PSU
- Third Crate/Backplane will be assembled at Stockholm and shipped to Mainz for w/b 18 March - fourth assembled and retained at Stockholm
- Two PSUs will be shipped to Mainz and Stockholm during March
- Sam has two new students starting work on adapting CP simulation software for the JEP system



UK Hardware Requirements -Slice Tests + Test System



<u>Module/card</u>	Needed	<u>Design/</u>	Manufacture/	<u>Number</u>	<u>Tested</u>	<u>Comments</u>
		<u>Layout</u>	Purchase	awaiting test		
DSS	10	-	0	6	4	Populates 1 full CPM (80 channels)
CMC LVDS Tx Card	20	-	16	0	4	} and 2 partial CPMs (40 + 40 channels)
CMC Generic I/O Card (GIO)	3	Layout	3	0	0	CPM-CMM tests via PB; CTP-D emulation
CERN TTC Test Card	4	-	0	0	4	Only usable on DSS - optical input
TTCdec Interposer	8	-	6	0	2	Needed to allow use of TTCdec with RODs
TTCdec	30	Design	20	7	3	Re-design needed for new TTCrx footprint
LVDS 4-channel Link Cable	126	-	0	0	160	15m - from 6 PPMs -> (2+2 CPMs + 2+2 JEMs) - from HD
СРМ	4	-	4	0	0	2 fully-populated, 1 partially-populated
CPM Emulator 1 (CPME1)	4	Design	4	0	0	Sources/sinks 160 Mbit/s serial data (firmware?)
CPM Emulator 2 (CPME2)	4	-	4	0	0	} Sources/sinks HIT data for CMM via PB
CMM Emulator (CMME)	2	Layout	2	0	0	} and provides CPM-CMM PB testing
СММ	4	-	4	0	0	2 for CP sub-system, 2 for JEP sub-system
Rear Transition Module	4	Layout	4	0	0	Sources/sinks CMM I/O data (crate dimensions awaited)
TCM/ALC	7	-	4	0	3	2 for UK, 2 for Heidelberg, 2 for Mainz, 1 spare
ROD <i>(6U)</i>	8	-	6	0	2	} Slice Tests - 3 for CP + 4 for JEP
CMC G-Link Rx Card	8	-	4	0	4	} sub-systems + 1 spare (CMM firmware needed)
S-Link Tx/Rx Card-set	7	-	1	0	6	Slice Tests RODs - 3 for CP, 4 for JEP
S-Link Rx PCI I/F	7	-	1	0	6	Slice Tests ROSs - 3 for CP, 4 for JEP
VME Mount Module (VMM)	5	-	4	1	0	Adapts 6U CPU to 9U VME crate - CP 2, JEP 2 + 1 spare
CPU (Concurrent)	6	-	2	0	4	Slice Tests - 2 VME crates + 4 VME crates
TTCvi + TTCvx	2	-	0	0	2	Slice Tests + UK Test System
6U VME crate	3	-	1	0	2	Slice Tests + UK Test System
9U crate/PB	2	-	0	2	0	} 1 for Slice Tests
9U crate PSU	2	-	0	0	2	} + 1 for UK Test System
Optical fibres (TTC + S-Link)	~15	-	~10	0	~5	Lengths?