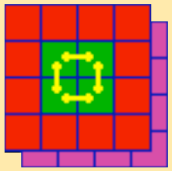
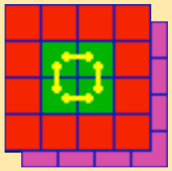


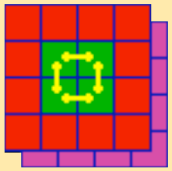
Rack, patch panel and cable layout

- Goals
  - Ease of access
  - Good cable mechanics
  - Specify lengths of short cables between patch panels and receivers, so they can be ordered
  - Minimise latency
  - Timescale: 1–2 months?
- Suggested procedure
  - Set up a small working party
  - Suggest and distribute a layout for comments
  - Incorporate comments in the solution



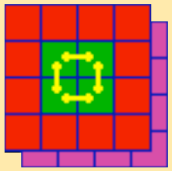
9U Readout Driver design

- **Goals**
  - Define specification for 9U ‘module-0’ ROD, leading to a Preliminary Design Review
  - Incorporate what we have learned so far, plus requirements of Preprocessor readout — *including compression of FADC raw data*
  - Probably cannot decide yet on processing requirements for calibration and monitoring — *make provision for processor or DSP daughter-board to be defined later?*
  - Timescale: 2–3 months?
- **Suggested procedure**
  - Set up a small working party
  - Invite all interested people to brainstorming session(s)
  - Write a draft specification



Latency reduction

- Goals
  - Summarise all present measurements
  - Define how to estimate or measure missing information
  - Consider possible areas for improvement:
    - rack and cable layout
    - board layout
    - choice of FPGA device types
    - firmware
  - Timescale: 2–3 months?
- Suggested procedure
  - Set up a small working party
  - Find out where we can and cannot gain significantly



Organisation

- Goals
  - Hardware coordinator's tasks: re-define *(also see below)*
  - Contact people: evaluate effectiveness, review definition of roles *(which contacts now needed, etc.)*
  - Coordinators: review structure needed for hardware, software, testing, …
  - Timescale: proposals by July meeting at Queen Mary
- Suggested procedure
  - Set up a small committee? *(Keep it light!)*
  - Talk to contact people and coordinators to get their views
  - Gather views from the community
  - Try to formulate solutions