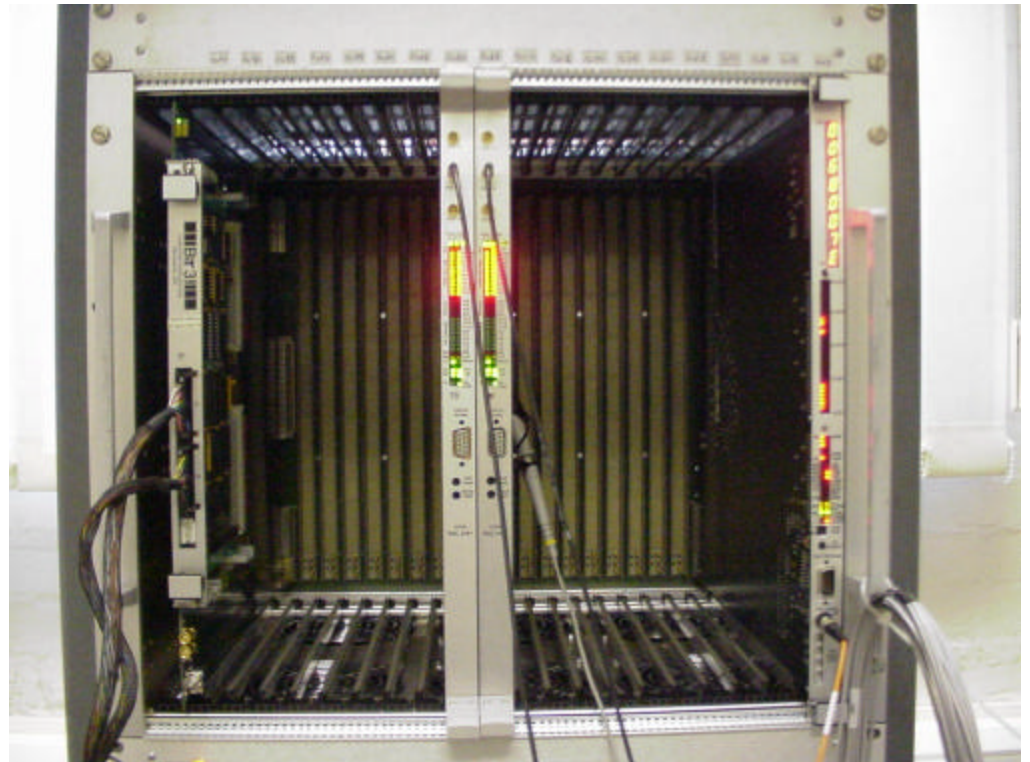


Cluster Processor Modules_ Testing

Uk Meeting, Thursday the 17th of April 2003

Cluster Processor Module #2

- 2nd CPM delivered:
 - 4 CP chips connected
 - All serialisers/ LVDS receivers working
- Mounted with new TTCdec card with I2C access
- TTC scan performed

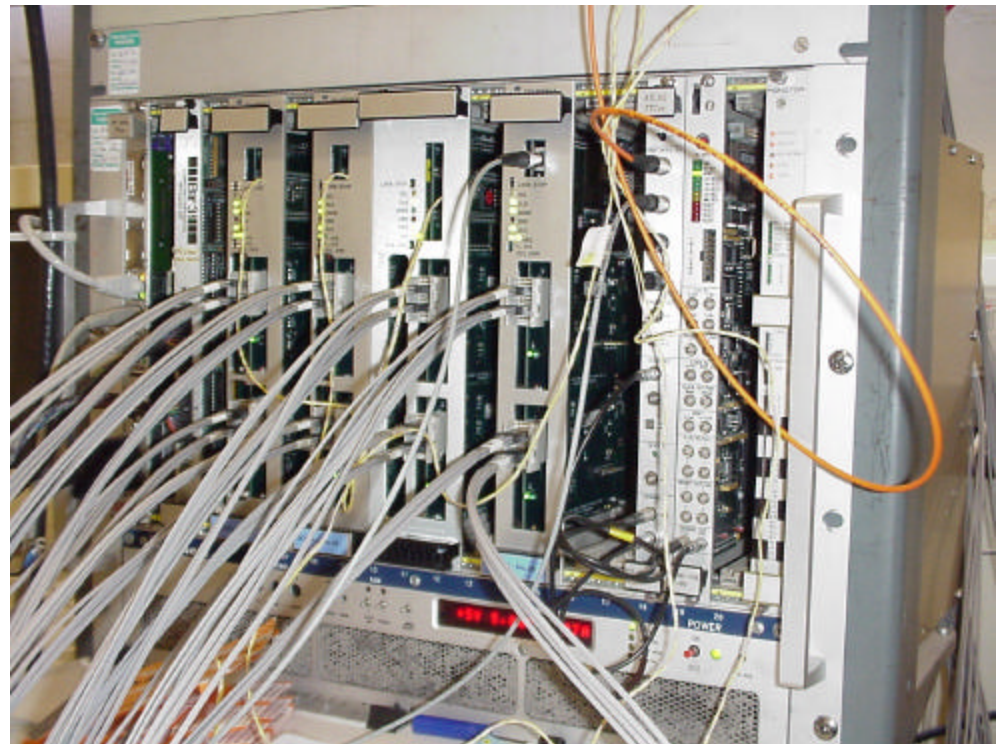


I2C Access Testing

- Provide virtual mapping of all I2C registers
- Hdmc part handles the formatting of data to perform I2C access according to Richard's scheme
- S/W modified to avoid using TTC broadcast
- It seems to work so far

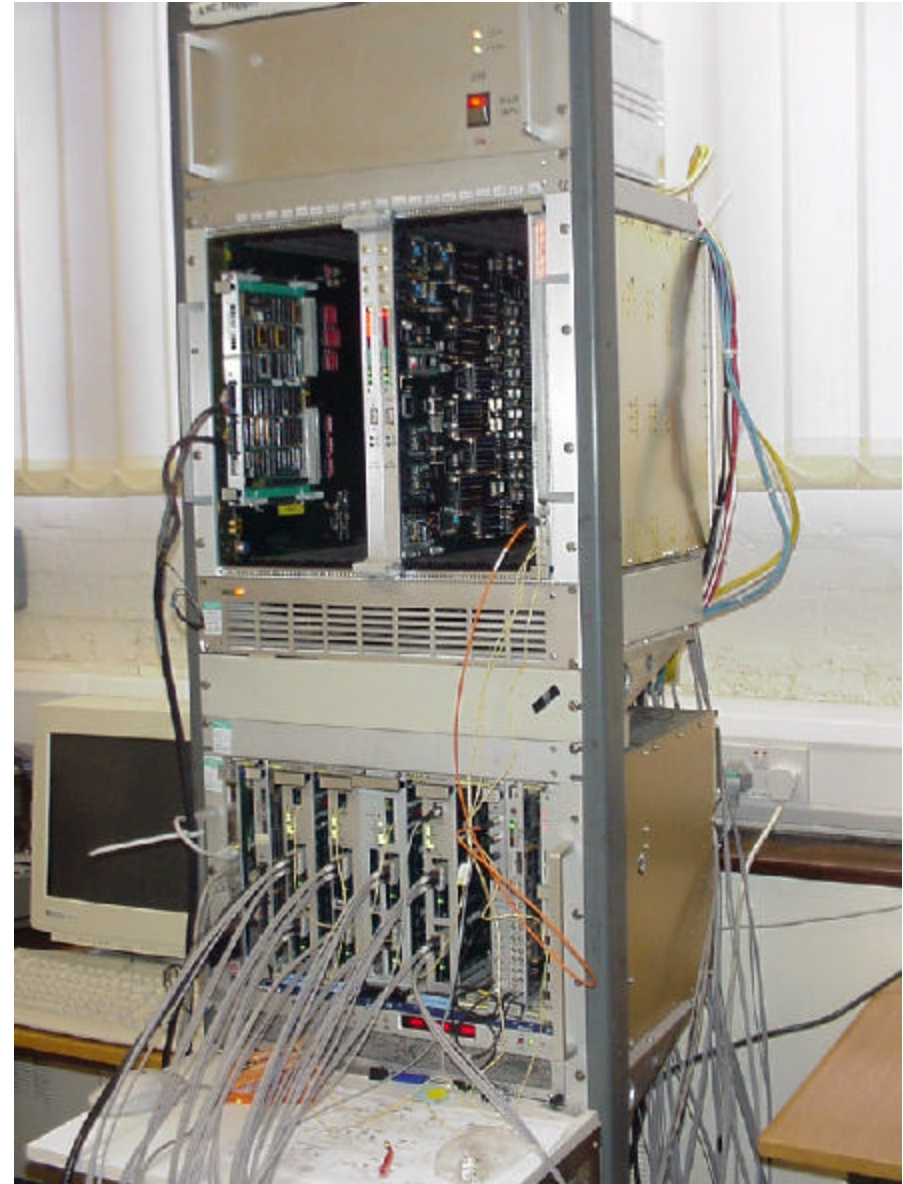
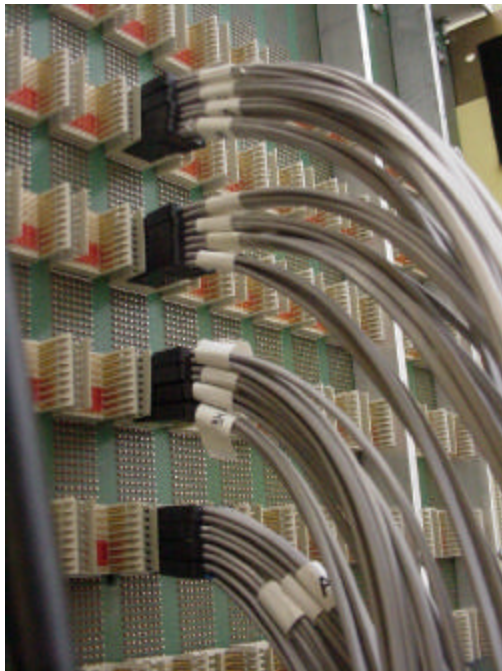
Three more Dss at B'ham

- 2 Dss were having damaged components:
 - Memory pins
 - Capacitors removed during mechanical insertion?
- On power-up of the crate, one Dss does not always load its f/w and clock not always on



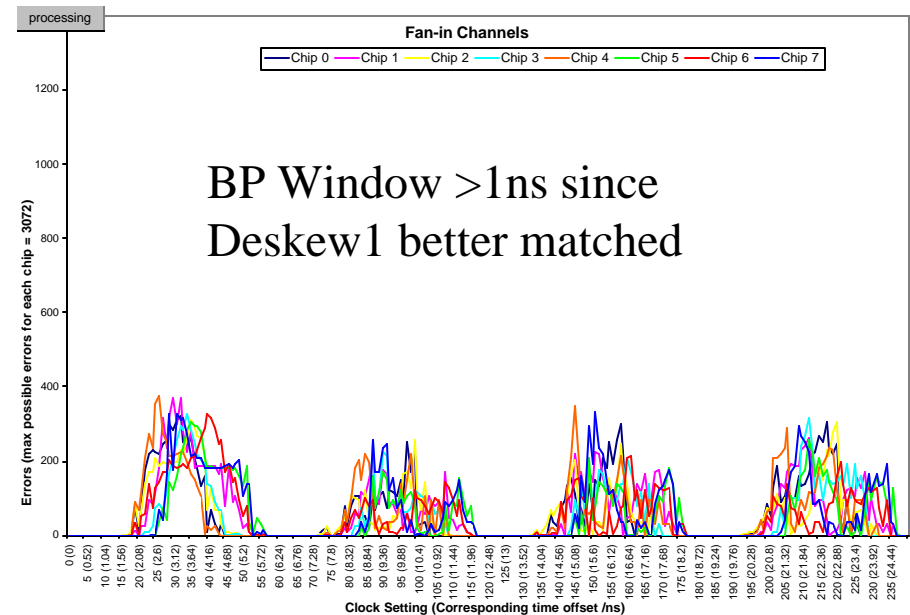
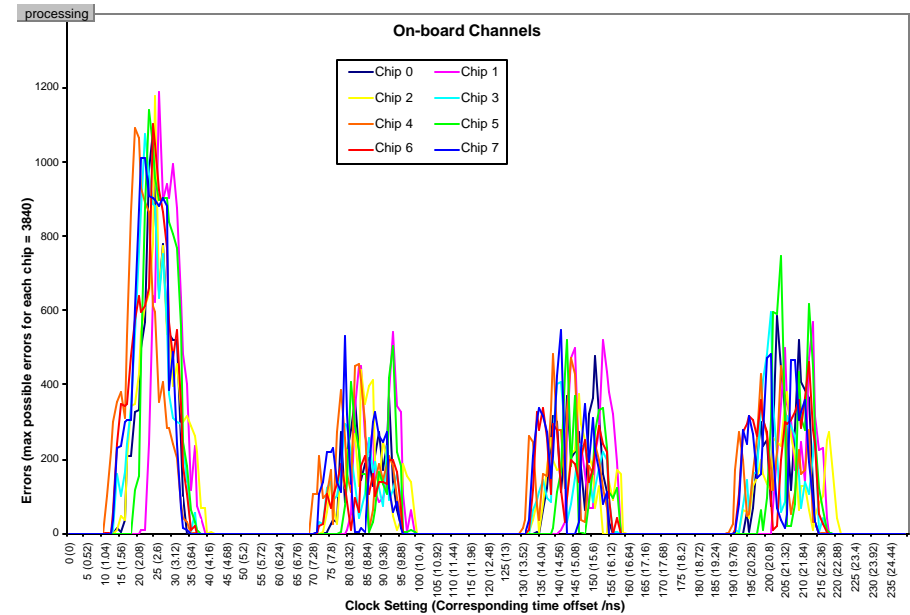
Full System Test

- 4 DSSs
- 2 CPMs
- 16 LVDS cables:



TTC Scan: CP chip Input

- Data are synchronized between 2 boards
 - Use of TTC Bcreset broadcast command to set pointer of all playback RAM at the beginning
- Data driving from left, then from right, to be re-done with same TTCdec
- Crosstalk studies
 - Cpm1: data source Dss
 - Cpm2: data source Ram
 - No crosstalk observed



Bit Error Rate Test

- F/W is working but with pseudo-random pattern of 128 length
- To scan all bits, need change design and try to use a random generator instead, identical to the one use in the DSS
- James sent random data generator code
- So far BER done overnight on 1 channel of 1 serialiser...no error seen!

Next Steps:

- Perform BER of both boards, checked for crosstalk
 - Scan the crate: very tedious...
- Test CP chip on CPM#2
- Synchronize Dss inputs (need same TTCdec card everywhere)
 - Test algorithm with Dss data
- Test the ROC
- Integrate with ROD
- Integrate with JEM?