CPM Prototype Hardware

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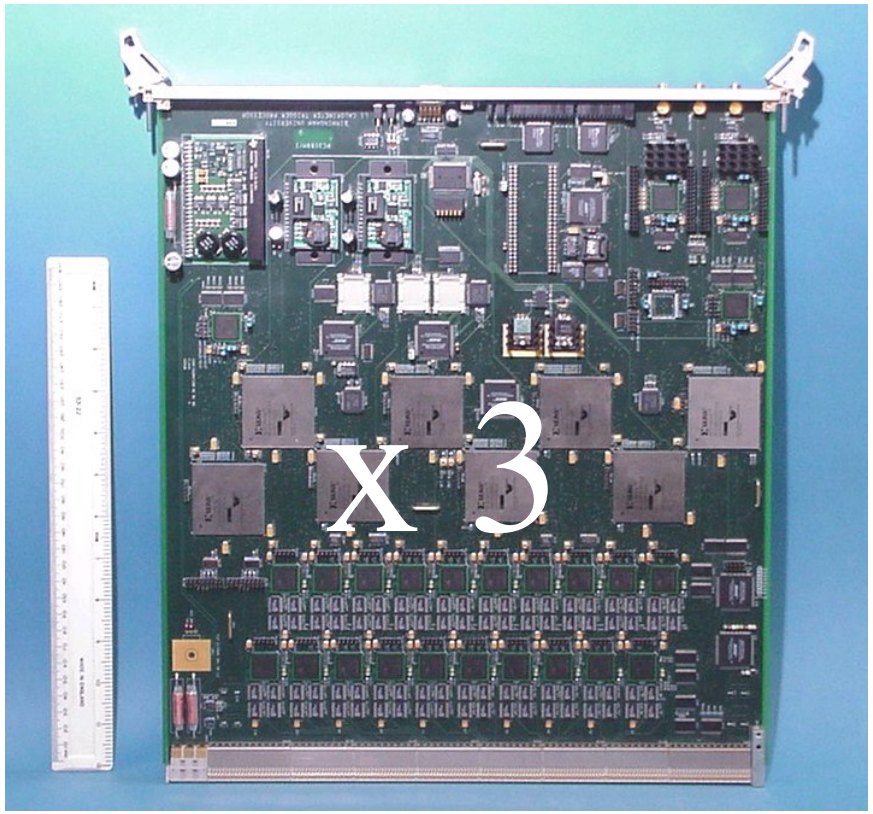

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Hardware Status

#1 - Assembled , fully working and in use at Birmingham for evaluation tests.

#2 - Assembled, but assembly defects with 4 CP FPGAs . Otherwise operational , and being used to drive data into #1

#3 - Just arrived. Needs preparation before JTAG testing.

#4 - ? will just contain Serialisers.

#3 & #4 were delayed - poor yield with 2nd run of PCBs.

TTCinputs

TCM outputs are series terminated (as specified).
CPM also had termination , effectively halving amplitude of signal. CPM resistor removed.

The series resistors on the TCM are the wrong value for a 100Ω differential line:
56Ω -> 39Ω

The biasing resistors also need to be lowered in value
560Ω -> 390Ω

Power Supplies

Birmingham PSU box modified:

3.3V supply turns-on after 5.0V supply.

Additional mains filter fitted

Powering-up no longer affects CPU crate.

Next Version

Recent Meeting it was decided to stay with present design using 8 VirtexE CP FPGAs per module.
Not enough time to develop a significantly different design using Virtex2 parts and SCAN-LVDS before the FDR.

Main Layout work will be to re-route the CP inputs from the backplane.

Aim is to keep other changes to minimum, and for module to be fully compatible with existing hardware.

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PCB Changes:

- Re-route CP backplane inputs , and check other FIO traces.
- Clock distribution. Timing must be tightly controlled.
  More PLLs to be added , 1 per CP Chip.
- Some Components to move for attachment of bracing-bars.
- All Virtex FPGAs configure from FLASH.
  Serial EEPROM will be removed.
- New TTCdec with different connector.

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- CP chip's unconnected Vref inputs to be used.

A simple change to Serialiser and CP FPGA firmware will enable SSTL2 signal levels to be used for FIO links.

Lower switching currents -> Less noise.

Better-defined thresholds -> improved timing margins.

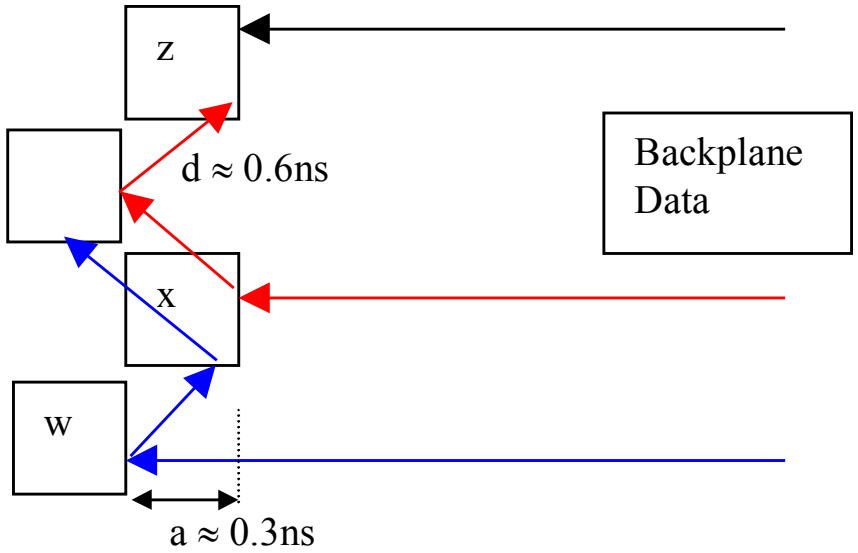
'Vref' version using existing firmware will be totally compatible with existing CPMs, having the same 2.5V I/O standard, so both versions will work together.

(Existing CPM may generate, but not receive, SSTL2 levels.)

CP FPGA Clocks

1 clock for onboard + ? clocks to capture backplane data)
(Onboard data arrives 2ns before data via backplane)

Geometry of present layout with 2 columns of CP chips:



Minimum skew due to transmission path differences are:

1 clock 1.2ns (2d)
2 clocks 0.9ns (a + d)
3 clocks 0.3ns. (a) x

Note:

- Not enough resources within the FPGA for 3 BP clocks
- Onboard signals already skewed by 0.7ns (2 columns of S.)

Timescales

- RAL DO available for CPM re-layout in July.
- Layout Modifications should be finished Mid-End August.
- Assembled boards (assuming PCBs OK) by October.

We must complete tests on present design before August.

ROC and HIT outputs have not been connected to real modules.

CPM CAN uC untested.

Summary

1 + ½ CPMs up and running. Another soon ?

Minor Design changes to CPM, retaining 8 VirtexEs.

New version by October,
to be debugged and tested by mid 2004.(FDR)