TTCrx Chip .vs. TTCrx Dec Card
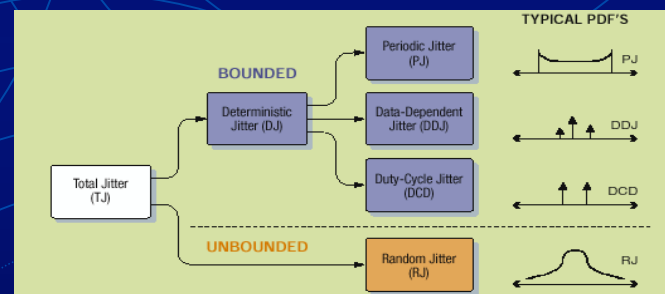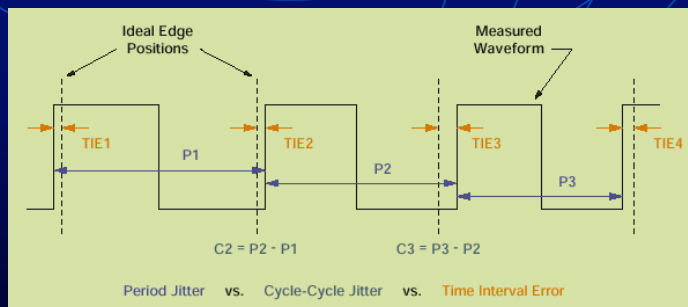## --Clock Jitter considerations

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What's jitter

- Jitter describes timing variation that occur more rapidly than Wander.
  - Threshold: 10Hz

- Jitter classification
  - Deterministic jitter (bounded)
  - Random jitter (Gaussian distribution, unbounded)

- Clock Jitter
  - Period jitter
  - Cycle-cycle jitter
  - Time Interval Error

Jitter???

- Why should we be concerned about jitter?
  - `Bit Error Rate`
- What are the meaning of the jitter requirements?
 - `300ps peak-peak?`
  - `150ps rms?`

Clock jitter & BER

- For random jitter, the ratio of peak value to standard deviation depends on the bit-error rate (BER) at which the system must operate.

- For BER $=10^{-12}$, Peak-Peak $= 14.262\sigma$

- Normally, the total jitter consists of both random jitter and deterministic jitter. The total jitter distribution is the convolution of the individual distributions.

| TABLE 1—GAUSSIAN-WAVEFORM PROBABILITIES	
BER	Ratio of peak deviation to standard deviation
1×10^{-4}	3.891
1×10^{-5}	4.417
1×10^{-6}	4.892
1×10^{-7}	5.327
1×10^{-8}	5.731
1×10^{-9}	6.109
1×10^{-10}	6.467
1×10^{-11}	6.807
1×10^{-12}	7.131
1×10^{-13}	7.441
1×10^{-14}	7.739
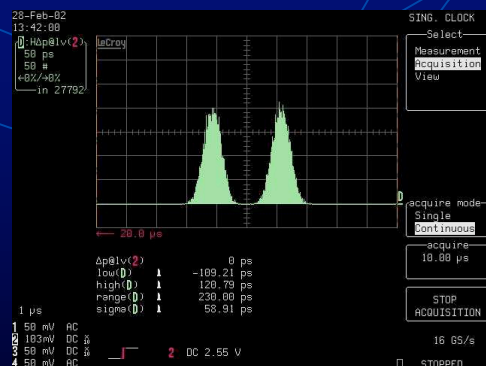
Clock Jitter Requirement

- According to Uli:
  - DS92LV1023
    - **RMS** jitter: *150ps*
  - The Virtex-II
    - Maximum cycle-to-cycle jitter: *300ps*
    - Maximum period jitter : *1ns*

- Questions:
  - Jitter requirement on G-Link?
  - Any other high speed link with jitter requirement?
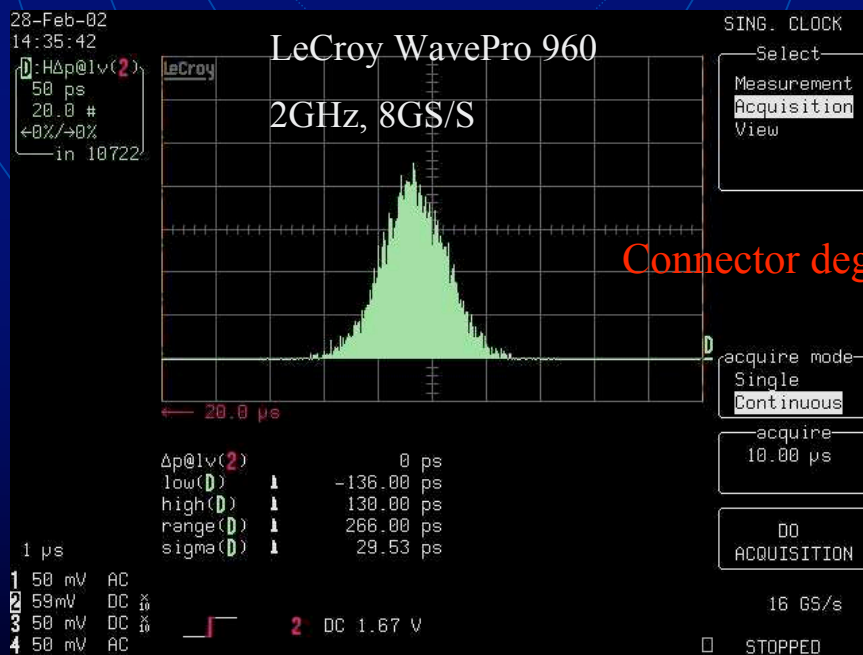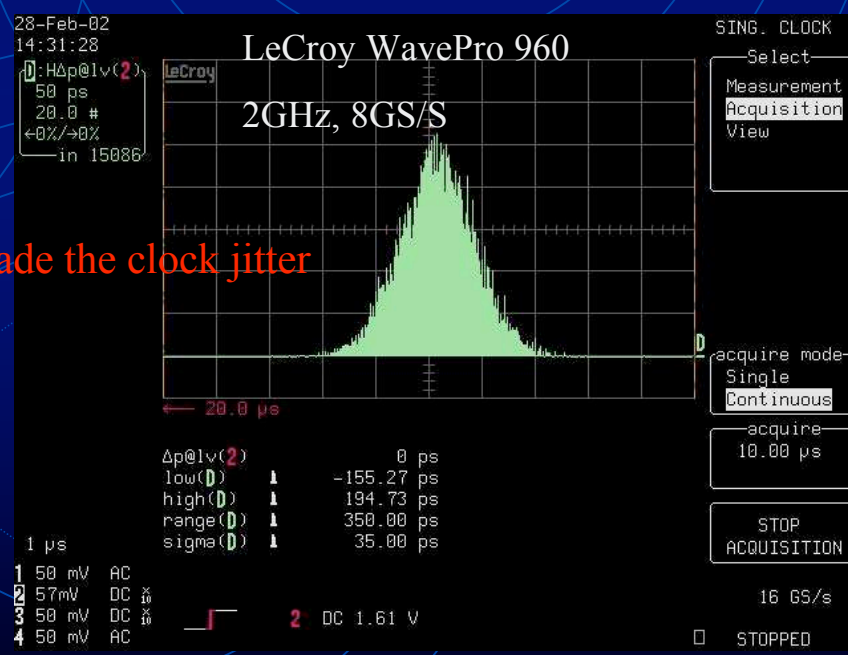 - What's the BER required for the system? 10^{-12}?

TTCrx & Dec Clock Jitter
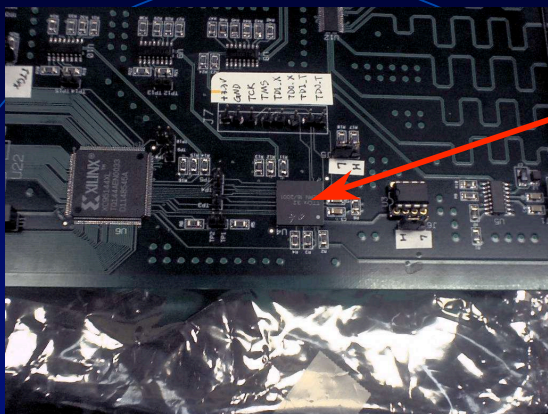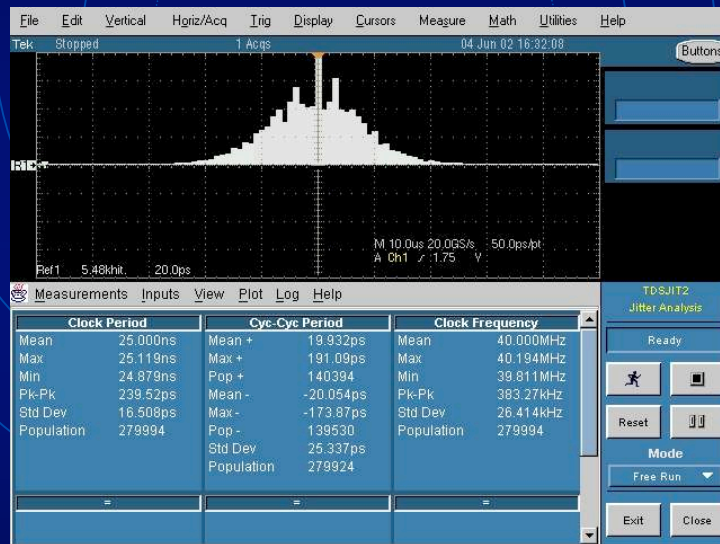

TTCrx Chip

TTCrx Daughter

LeCroy WavePro 960

2GHz, 8GS/S
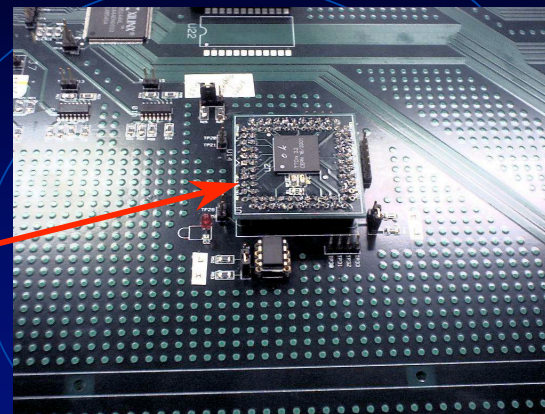
Connector degrade the clock jitter
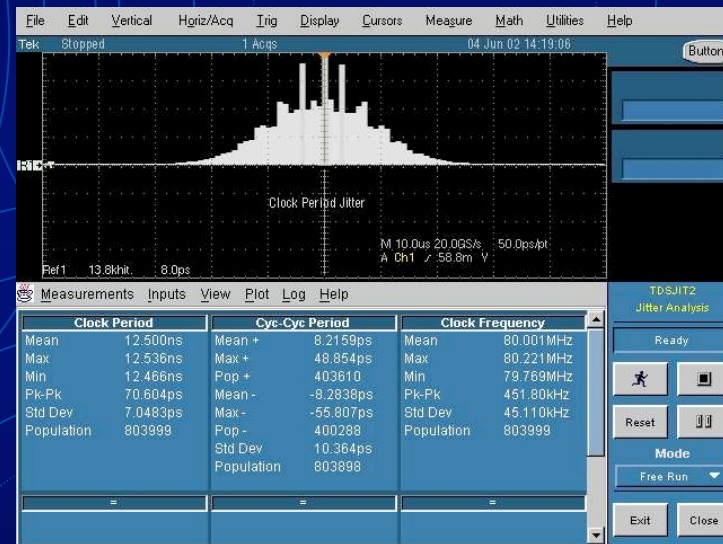
LeCroy WavePro 960

2GHz, 8GS/S

PLL Clock Jitter

- Clock jitter at TTCrx chip output
- Clock jitter at PLL MPC992 output

Tektronix 7254, 2.5GHz, 20GS/S

Some considerations

- PLL Clock frequencies(40MHz, 80MHz, …)
- Cleaned Clock distribution
  - Signal level: LVDS or PECL?
  - Connector, cable, termination
- TTCrxDec connector impedance, reliability
- fpBGA assembly problem, Cost for TTCrxDec, ……
- What if we, in future, will want to upgrade the G-Link speed from 800M to 1.6G, which will put a more strict jitter requirement on the Clock? Shall we leave some headroom for this when deciding our jitter budget now?
- Jitter test and BER test in future.

Conclusion

- It is difficult to define the jitter requirements clearly.
- Minimize the clock jitter as possible as we can.
  - Proposed approach:
    - Put TTCrx directly on main board.
    - Put PLL on main board where the clean clock is to be used.
    - Convert single-end TTCrx CMOS clock into differential signal near the TTCrx chip and transmit to PLL.
  - Compromised approach:
    - Put TTCrx on TTCrxDec.
    - Put PLL on main board where the clean clock is to be used.
    - Convert TTCrx CMOS clock into differential signal on TTCrxDec.
    - Choose better connector for TTCrxDec.
    - Solder TTCrxDec directly on main board.
  - Possible approach:
    - Put both TTCrx and PLL on TTCrxDec.
    - Use differential signal for clean clock.
    - Choose impedance controlled surface mount connector for TTCrxDEC.
    - Solder the TTCrxDec directly on main board.
    - On main board, routing the clean clock far from other high speed signal lines.

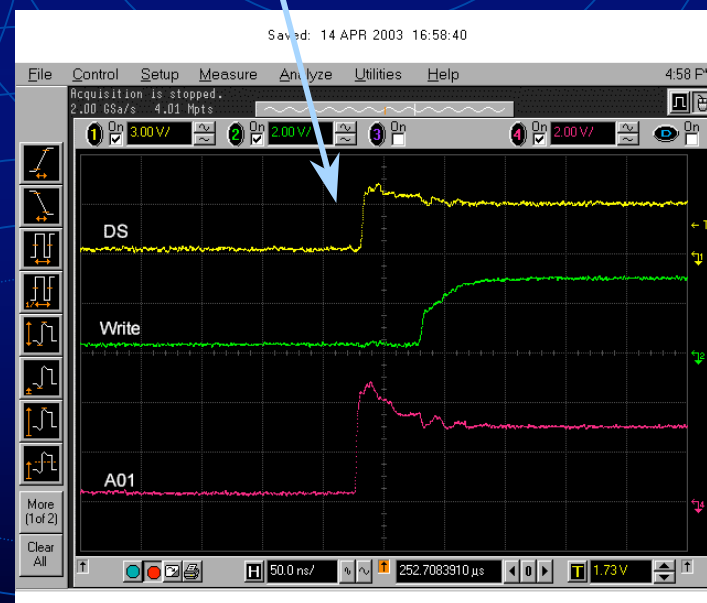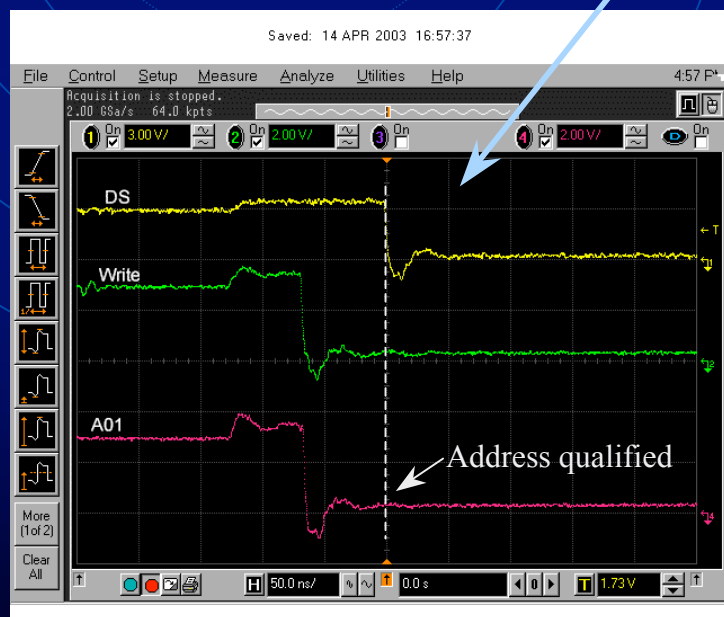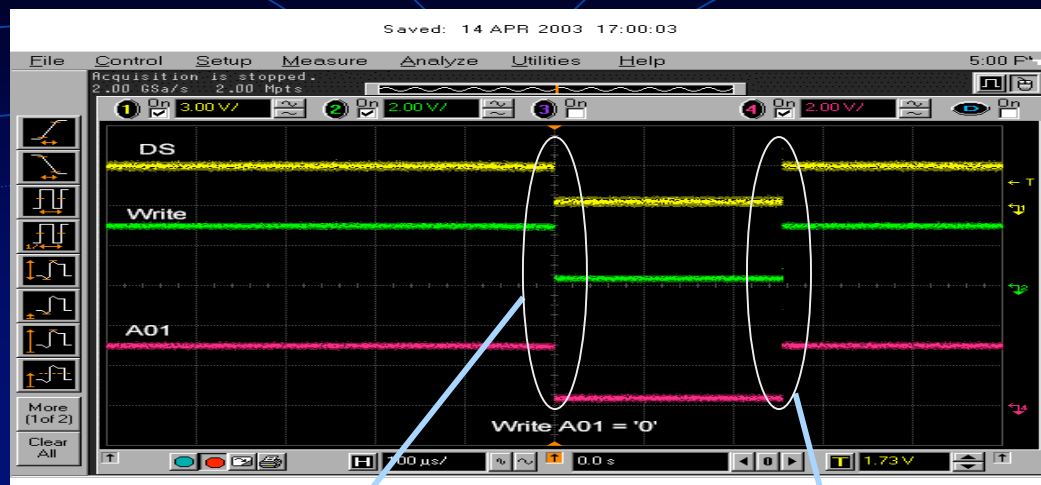# VME– signal test on Processor Backplane

W. Qian

Test Setup

- Custom 9U VME Crate

- CPU board in slot 2

- TCM in slot 21

- All other slot are empty

- Agilent Infinium 54832D, 1GHz, 4GS/S
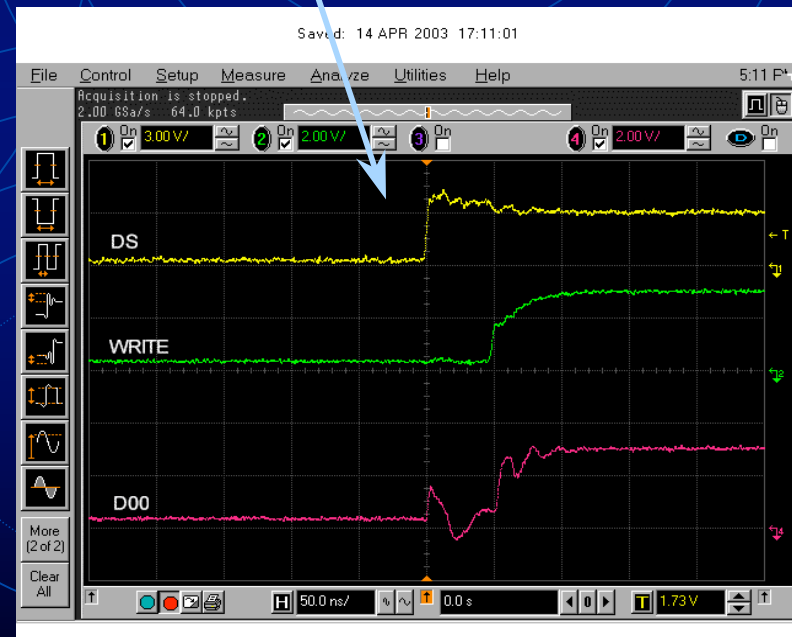
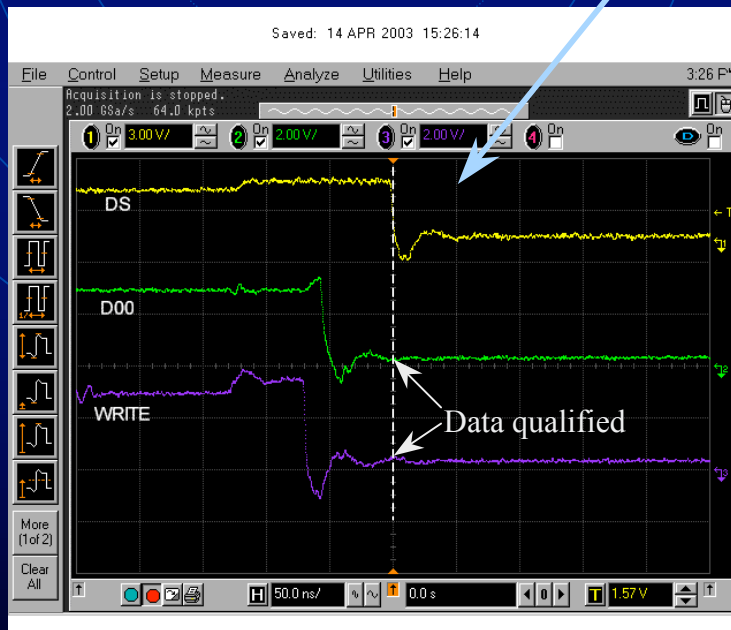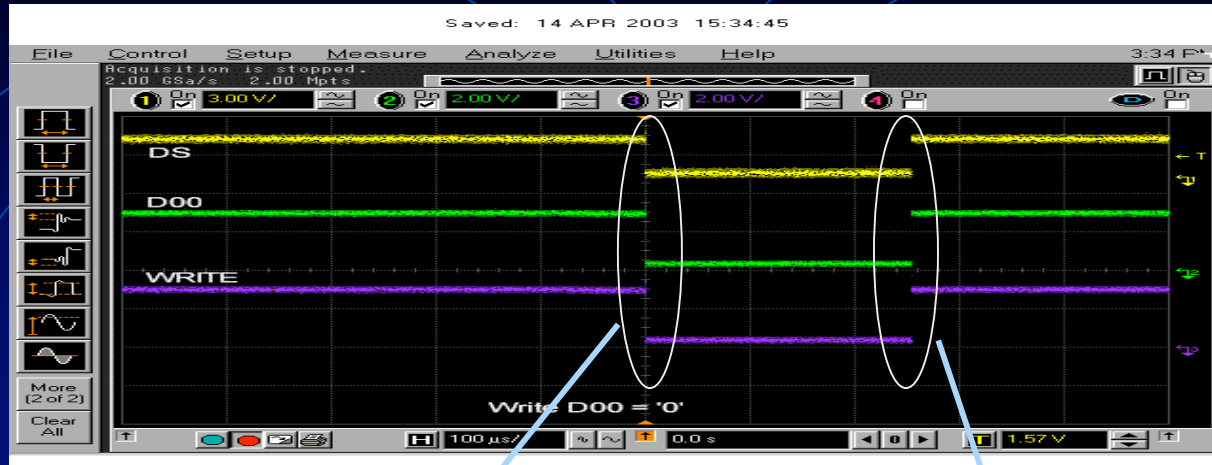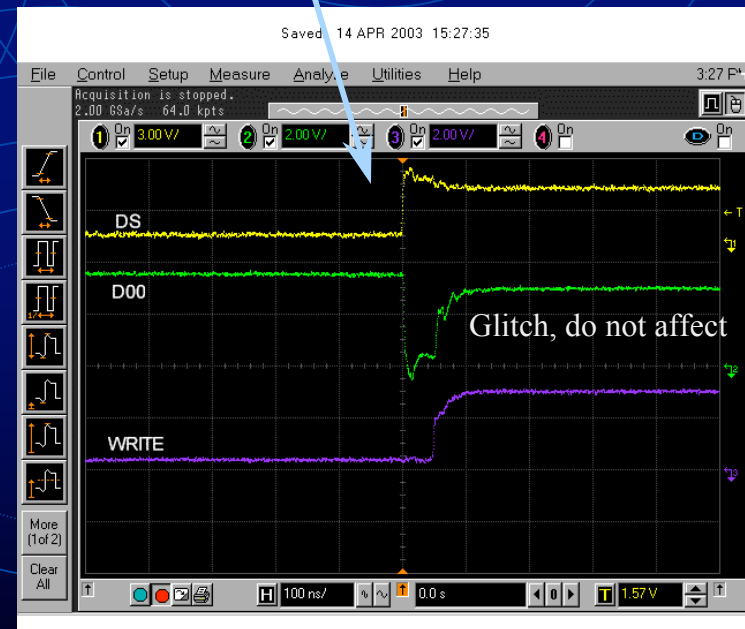- Signals probed on the back connector of TCM
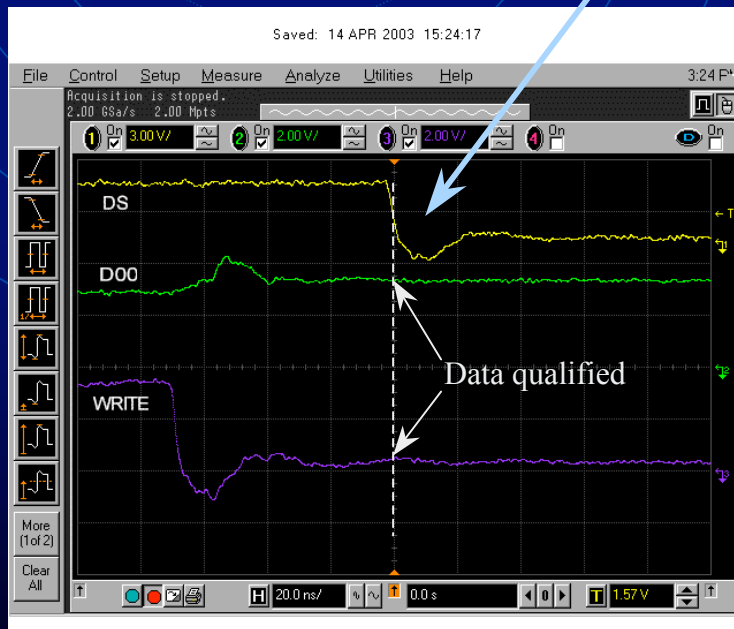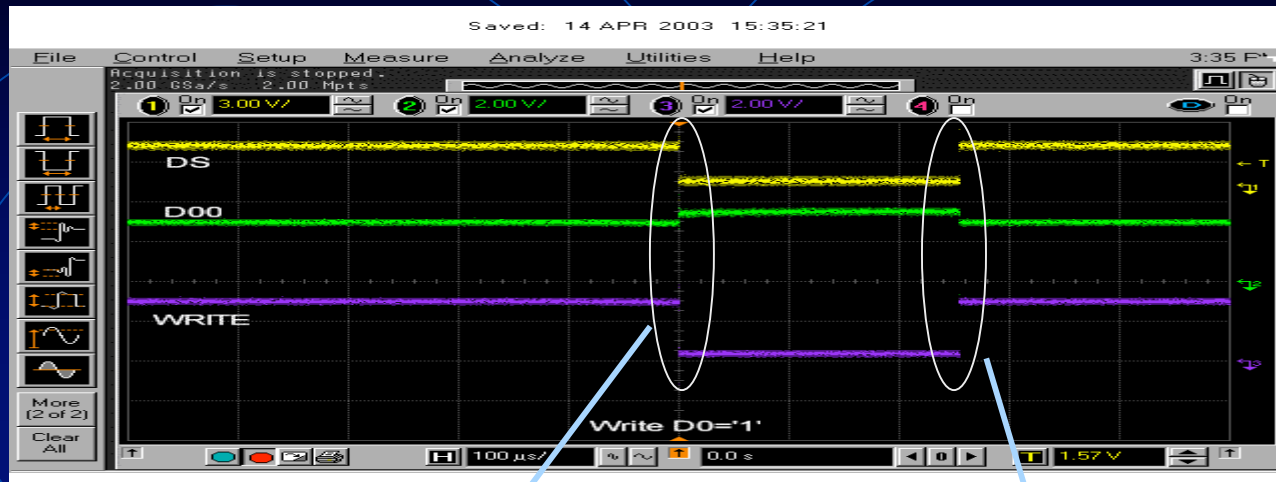
Address line

ATALS L1 Meeting - RAL

Data lines

Data lines

Conclusion

- VME– signals on the 9U custom backplane seem good at present set up. Overshoot ~ 30%, undershoot ~10%.

- When most of the slots are to be populated in future, the capacitance of the signal trace on the backplane will increase, then the impedance will decrease, so the reflection(overshoot, undershoot) will be higher.

- More test will be needed when the 9U crate is fully populated.

VMM Status

W. Qian

- All VMM's are working now.
- VME64 Power Supply Parameter
  - +5V
    - Max 5.250V
    - Nominal 5.000V
    - Min 4.875V
- CPU board Power Supply Requirement
  - +5V
    - Regulation +/-5%
    - Max 5.250V, Min 4.750V

- **Problem**
  - Fuse resistance causes a significant voltage drop ~ 150mv

- **Solution**
  - Use a thick copper wire to short the fuse
  - Use a low resistance fuse