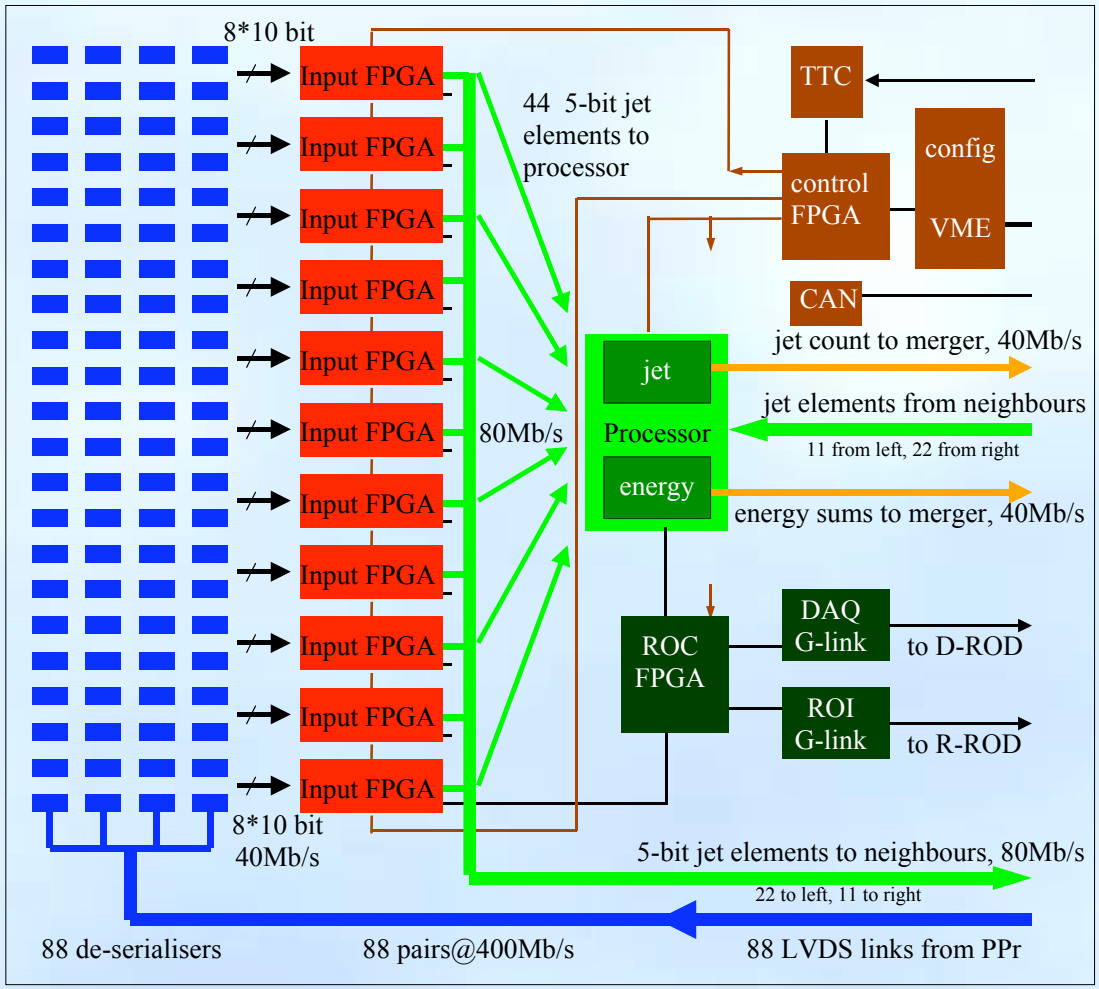
19th May 2003

JEM tests

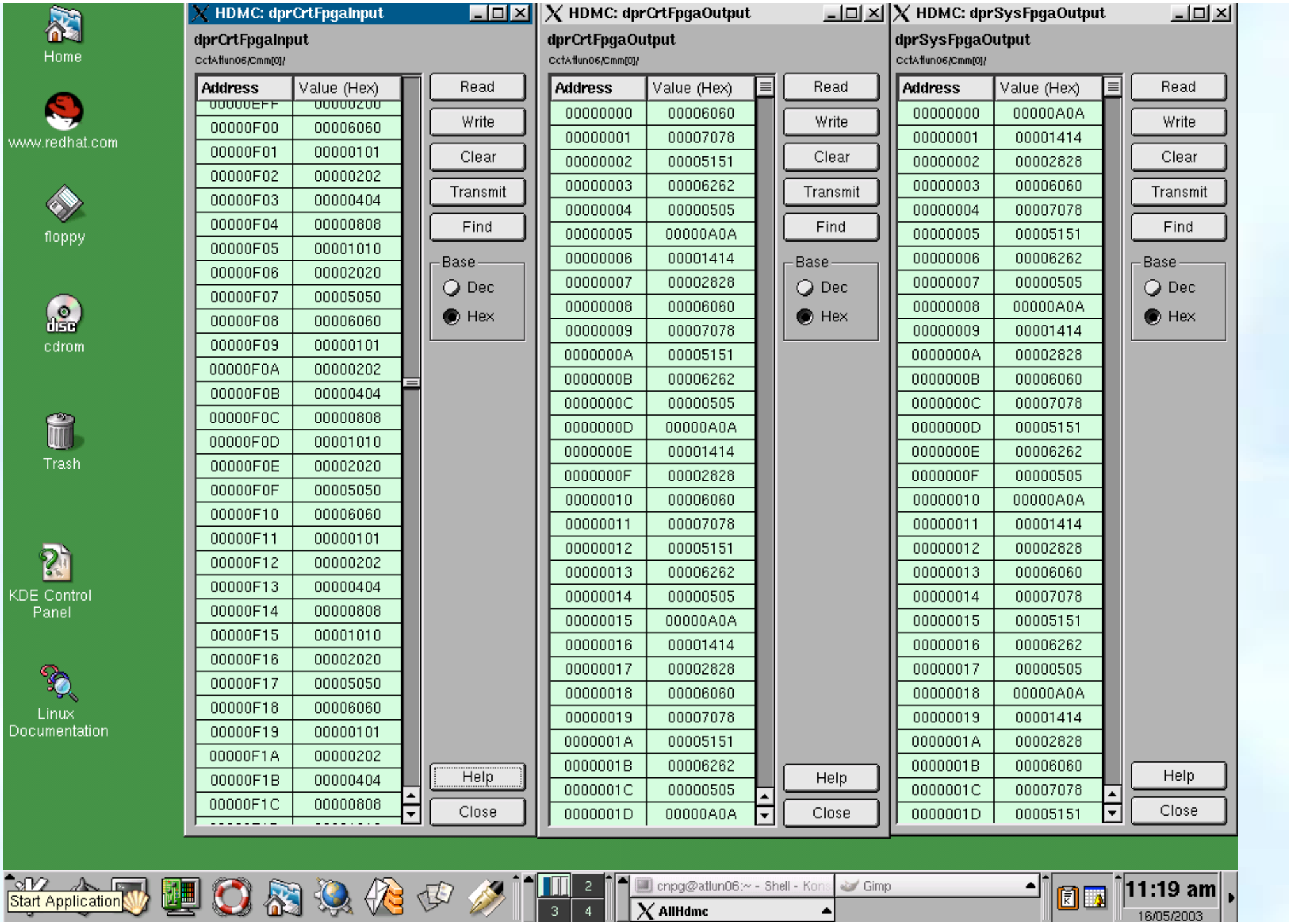
C .N .P .Gee
Rutherford Appleton Laboratory

Jem


8*10 bit
Input FPGA
Input FPGA
Input FPGA
Input FPGA
Input FPGA
Input FPGA
Input FPGA
Input FPGA
Input FPGA
Input FPGA
8*10 bit
40Mb/s
44 5-bit jet elements to processor
80Mb/s
TTC
control FPGA
config
VME
CAN
jet count to merger, 40Mb/s
jet
Processor
energy
jet elements from neighbours
11 from left, 22 from right
energy sums to merger, 40Mb/s
ROC FPGA
DAQ G-link
to D-ROD
ROI G-link
to R-ROD
5-bit jet elements to neighbours, 80Mb/s
22 to left, 11 to right
88 de-serialisers
88 pairs@400Mb/s
88 LVDS links from PPr

Jem Status

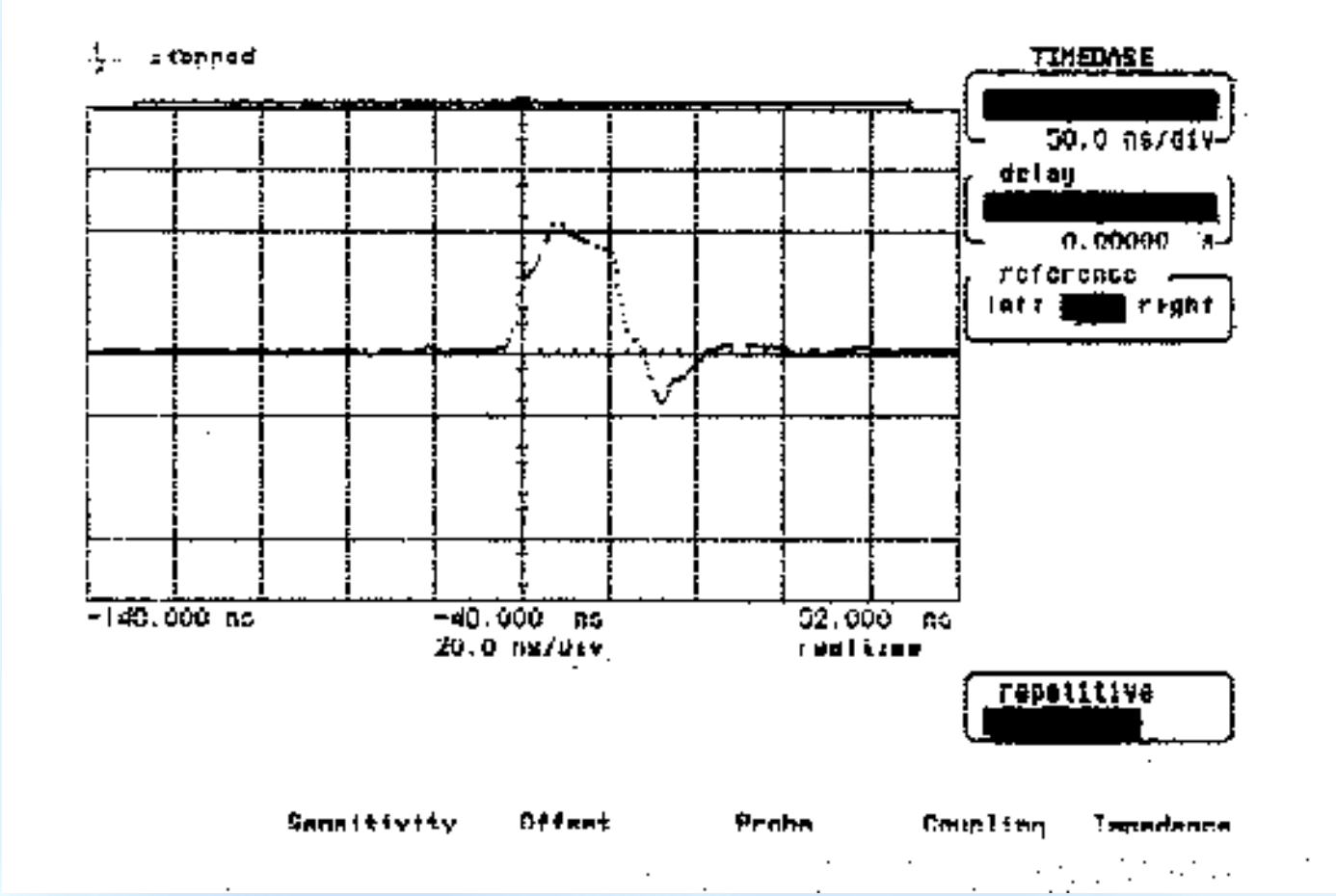
- **Jem 0.2 has larger main FPGA than Jem 0.1**
- **Modules communicate over backplane (last time).**
- **This time – first attempt to run Jet & Energy Code.**
  - Confusion over ordering of nibbles between Input & main FPGA.
  - And about convention for clocking data into main FPGA.
  - Problems with registers in combined design.
- **Second attempt to run with CMM**
  - Tried with 1 and 2 JEMs (See Ian's talk).
- **Second attempt to run with ROD**
  - Single Jem (See Bruce's talk)


Home
www.redhat.com
floppy
cdrom
Trash
KDE Control Panel
Linux Documentation
HDMC: dprCrtFpgaInput
dprCrtFpgaInput
CctAtlun06/Cmm[0]/
Address
Value (Hex)
00000F00 00006060
00000F01 00000101
00000F02 00000202
00000F03 00000404
00000F04 00000808
00000F05 00001010
00000F06 00002020
00000F07 00005050
00000F08 00006060
00000F09 00000101
00000F0A 00000202
00000F0B 00000404
00000F0C 00000808
00000F0D 00001010
00000F0E 00002020
00000F0F 00005050
00000F10 00006060
00000F11 00000101
00000F12 00000202
00000F13 00000404
00000F14 00000808
00000F15 00001010
00000F16 00002020
00000F17 00005050
00000F18 00006060
00000F19 00000101
00000F1A 00000202
00000F1B 00000404
00000F1C 00000808
Read
Write
Clear
Transmit
Find
Base
Dec
Hex
Help
Close
HDMC: dprCrtFpgaOutput
dprCrtFpgaOutput
CctAtlun06/Cmm[0]/
Address
Value (Hex)
00000000 00006060
00000001 00007078
00000002 00005151
00000003 00006262
00000004 00000505
00000005 00000A0A
00000006 00001414
00000007 00002828
00000008 00006060
00000009 00007078
0000000A 00005151
0000000B 00006262
0000000C 00000505
0000000D 00000A0A
0000000E 00001414
0000000F 00002828
00000010 00006060
00000011 00007078
00000012 00005151
00000013 00006262
00000014 00000505
00000015 00000A0A
00000016 00001414
00000017 00002828
00000018 00006060
00000019 00007078
0000001A 00005151
0000001B 00006262
0000001C 00000505
0000001D 00000A0A
Read
Write
Clear
Transmit
Find
Base
Dec
Hex
Help
Close
HDMC: dprSysFpgaOutput
dprSysFpgaOutput
CctAtlun06/Cmm[0]/
Address
Value (Hex)
00000000 00000A0A
00000001 00001414
00000002 00002828
00000003 00006060
00000004 00007078
00000005 00005151
00000006 00006262
00000007 00000505
00000008 00000A0A
00000009 00001414
0000000A 00002828
0000000B 00006060
0000000C 00007078
0000000D 00005151
0000000E 00006262
0000000F 00000505
00000010 00000A0A
00000011 00001414
00000012 00002828
00000013 00006060
00000014 00007078
00000015 00005151
00000016 00006262
00000017 00000505
00000018 00000A0A
00000019 00001414
0000001A 00002828
0000001B 00006060
0000001C 00007078
0000001D 00005151
Read
Write
Clear
Transmit
Find
Base
Dec
Hex
Help
Close
Start Application
2
3
4
cnpg@atlun06:~ - Shell - Kons
Gimp
AllHdmc
11:19 am
16/05/2003

General Comments

- **Most of the time went in Firmware and Software work:**
  - Can't change main FPGA firmware from RAL
    - ***Either need suitable machine at Stockholm or Mainz…***
    - ***…or at RAL with appropriate software.***
  - Need better preparation for software integration
    - ***Complex (time-consuming) to get database & system dependencies correct***
    - ***Start visit with software experts only?***
- **Hardware generally started much quicker**
  - E.g. links up within 12 hours, cf 4 days last time.
  - Jem 0.1 still unstable, Jem 0.2 seems more robust.
- **Improved infrastructure in Lab 12 makes life much easier.**

Backplane


TIMEBASE
50.0 ns/div
delay
0.00000 s
reference
left right
-40.000 ns
20.0 ns/div
repetitive