CMM hardware and firmware status

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- Firmware: CP, JE
- CMM #1 status
- CMM #2 status

CMM Firmware

- CPM hit counting:
  - VME address map modified to provide better correspondance between CP, JE & JH versions
  - Change requests flowing back from subsystem tests....

- Jet Energy Summing:
  - built around real-time algorithm block designed by Andrea Dahlhoff
  - Design completed; functional tests completed.
  - Crate FPGA: timing simulation finished. Latency = 2 BCs + 4 ns
  - System FPGA: doesn't yet work at 40 MHz. Development continues....

- Jet hit counting:
  - To be produced by Sam Silverstein, who received CP hit code in March.

CMM # 1: subsystem tests

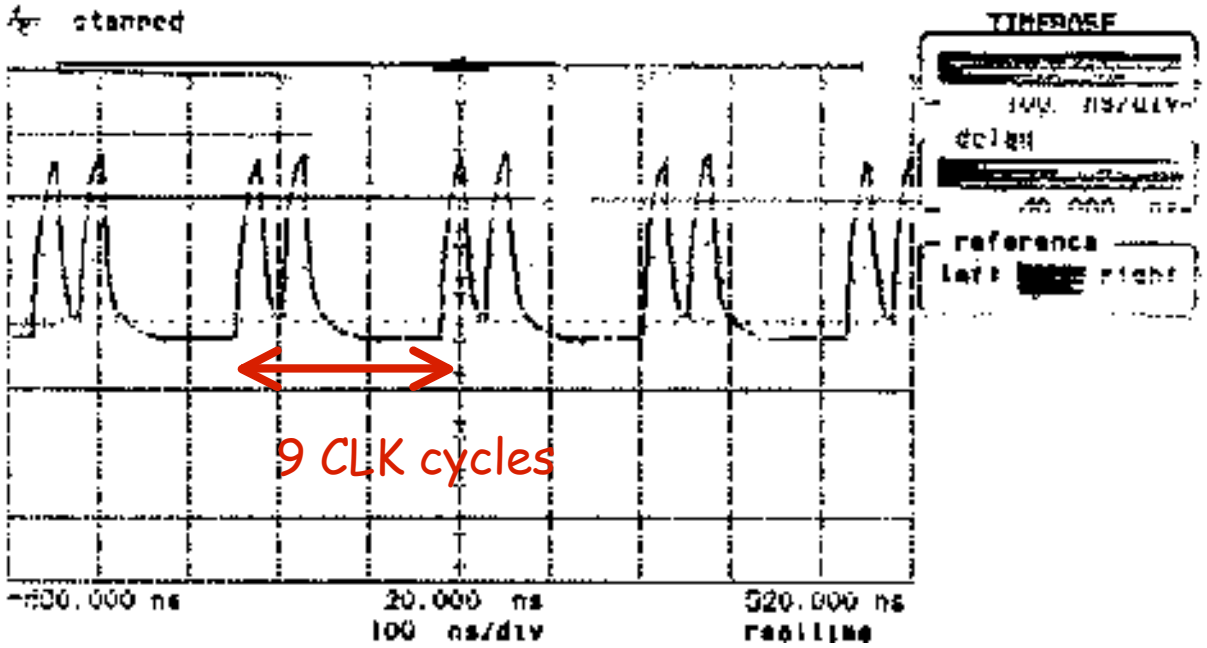
- CMM #1 run in a Crate with 2 JEMs

- JE firmware not ready so CP firmware used: internal processing of data is different but required IO functionality is there.

- Data from both JEMs seen correctly at CMM inputs
- Sum of data recorded correctly in RAMs at Crate-logic output & System logic output (according to CP functionality)
- Data seen on scope at CMM front-panel output (to CTP).

- data transmitted successfully across backplane (14 slots)
- no parity errors seen for few minutes running
- first time 2 sources external to CMM have been summed.

CMM # 1: output sketch



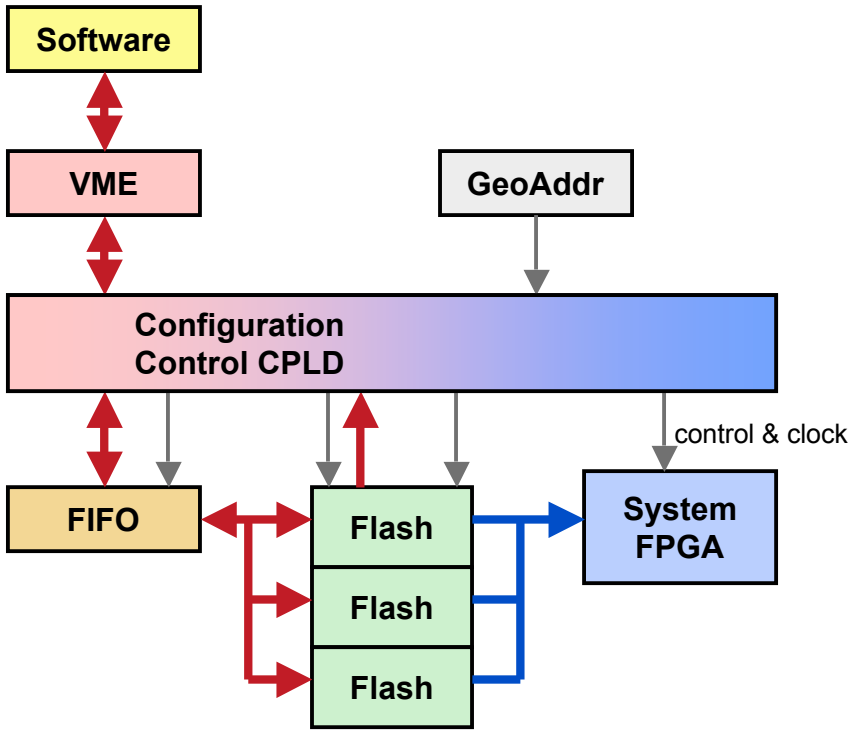
- Unterminated LVDS signals - ignore shape
- Pattern repeats with expected frequency

CMM # 2: Status Overview

- CMM #2: designed to correct mistakes in original CMM, mainly schematic error which disabled auto-config of Crate FPGA.
- 5 PCBs manufactured; 1 assembled:
- Boundary scanned with no errors.
- VME interface tested: works OK.
- Made a start testing real-time path.
- Priority has been to test auto-configuration logic:
  - this area was never fully tested on CMM #1 (CPLD problems. lack of software).
- Testing on hold during subsystem tests (crate shortage).
- Schedule:
  - aim to finish RT-path & ROD-path tests in 3 weeks, and then send out remaining PCBs for manufacture.

CMM # 2: FPGA Configuration Logic

- Commissioned by Panagiotis & Niel Falconer....
- Neil written Labview interface to load Flash RAMs via VME.
- 5 Xilinx config files successfully written / read to CMM (fill 2.5 Flash RAMs)
  - transfer takes 12 min / file
- System FPGA configures on power-up or request
- Geographic address determines which config file is loaded in FPGA.
- Need to double-check results but looks as if everything works for Sys FPGA.
- Config logic for Crate FPGA is exact replica so that should work too.



Summary

- Work continues on JE firmware
- CMM #1 has been used successfully in subsystem tests with JEM
- Most important test for CMM #2 - auto-config logic - has been passed successfully.
- Aim to finish testing CMM #2 within 3 weeks and send out rest of PCBs for assembly.