Cluster Processor Modules Testing

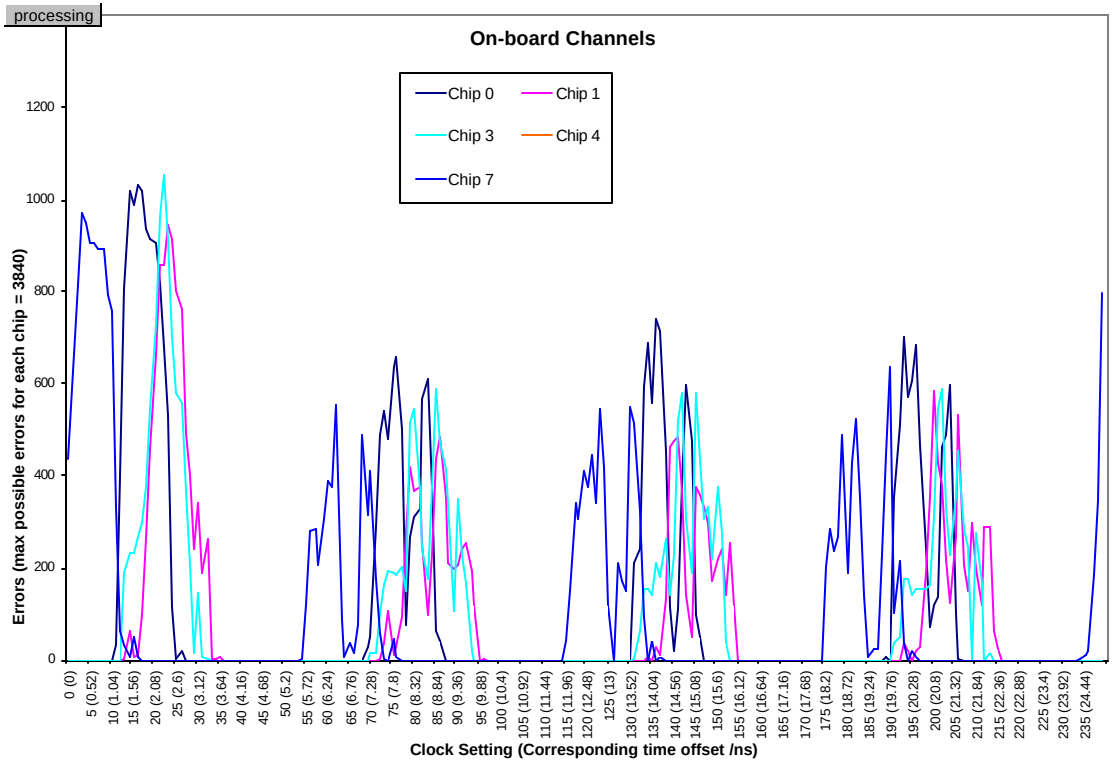
Uk Meeting, Thursday the 19th of May 2003

Cluster Processor Module #1

- BER performed on 16 Serialisers:
  - Overnight run without errors: 10^{-13}
  - Not with a pseudo random pattern
- 1.8V power convertor failed
  - Don’t know when it has happened
    - Downloading FlashRam?
    - Downloading Fpga?
  - 1.8V is the supply of Fpga
  - Replaced with power convertor of CPM #2

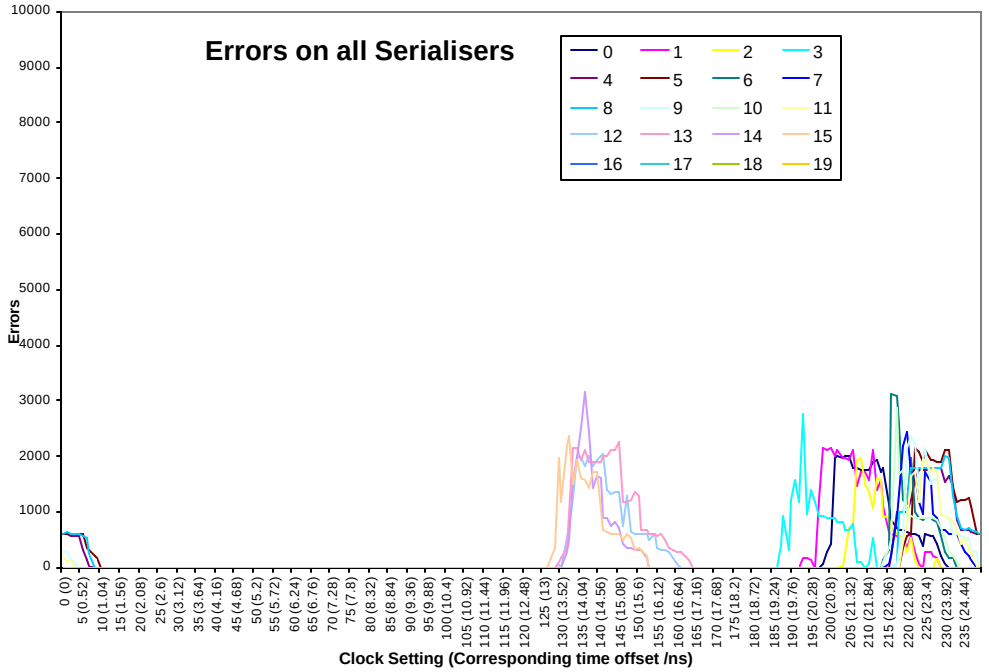
Cluster Processor Module #2

- 5 CP chips working (not grouped)
- TTC Scan shows wider window as the clock has not been routed



DSS Deskew1 Adjustment

- Time_reg available to adjust phase of main Clock or Deskew1 or Deskew2, per 1 ns step
- So far seems to ignore the step value
- But the option is there!



CPM#1 Integration Test

- Crate 1:
  - 1 VMM + 1 Cpu Board
  - 1 CMM
  - 1 CPM
  - 1 TCM
- Crate 2:
  - 1 Dss + 2 DB Lvds
  - 1 Rod
  - 1 Dss + Slink card
  - 1 TTC system

Integration Test: stand-alone test

- Transfer data between Srl Playback and CP chip in ScanPath mode
  - Cp chips behave oddly: ScanPath Fifo does not reset correctly but data are ok
  - After 1-2 minutes run, F/W DONE signal goes down: a CPM reset is triggered somehow
  - CP algorithm: data available in CP Dual Port Ram and Hit output does not make sense

Integration Test: with DSS and LVDS DBs

- Lvds Rx locked correctly
- Data correctly recovered in spy memory
- TTC scan performed correctly

Integration Test: with 1 Rod

- Several 1-slice DAQ data are sent from CPM to 1 Rod input
- Glink locked – DAV signal correctly delivered
- Several 1-Slice Data recovered at least on one Rod input channel, with right length (84 bits):
  - Don’t know yet if data make sense though
- Problems seen:
  - Length of Data wrong as soon as rate of L1 is too high
  - Only 1 channel (among 4 on G-link receiver) seems to work at low rate

S/W update

- Created environment to run at RAL: CpSliceTest
- RunControl Panel delivered Status on Cpm
- F/Ws are loaded now from DataBase
- RH7.3 to be installed

Next Steps:

- At RAL:
  - Understanding behavior others channels of Rod: investigate timing issues? ChipScope on input?
  - Increase rate of L1
  - Sent data to 1 CMM
- At B’ham
  - Set VMM with one Cpu (no more Bit3)
  - Repeat stand alone tests
  - Identify Reset Generation and F/W behavior

Thank you to

- Murrough, Norman, Bruce, Uli, Thomas, Attila, Cano