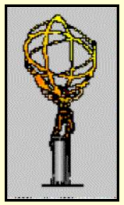

Latency

- **Proposed to form a small Latency Working Group –**
  - There are worries about the apparent increase in L1 latency – first noticed in the CP sub-system
  - Task will be to assess the current latency budget, and examine every element which contributes to it for possible reductions
  - Areas where savings could possibly be made include:

    Cabling *(including patch-panels)*

    Algorithms *(implementation in firmware and specific FPGAs)*

    Interfaces *(links between sub-systems, data capture along pipelines, clocking, etc)*
  - Probably last opportunity to make improvements – final module designs just started
- **Interested people are:**
  - Paul, Murrough, Gilles, Uli, Sam, Tony
- **First meeting – phone conference on Wednesday 21st May**
  - Define strategy, divide out tasks, propose some deadlines