Progress/Status January 2003

- CP and Serialiser FPGA Firmware
- Prototype ROD
- CMM
- TCM, VMM, TTCrx, etc
- Test Modules
- Others

Progress/Status January 2003

- **CP and Serialiser FPGA Firmware**
- **Firmware design demonstrated to interested parties last week**
  - **No problems with the Serialiser Firmware so far!**
  - **CP Firmware**
    - **problem with the clock calibration logic (160 MHz)**
    - **Multiplexed four clock phase solution does not work**
    - **Two phase solution is tried now**
    - **Virtex E (current) does not have sufficient global resources**
      - **to Distribute the clocks on global nets**
      - **and to multiplex the data**
    - **Future**
      - **target a new design for the Virtex 2**

Progress/Status January 2003

- **Prototype ROD**

Firmware	Status	Test	Comments
CPRoI	Done	Extensive tests in R1 Lab	ROD-DSS Test Completed
CP Slice	Done	Extensive tests in R1 Lab	ROD-DSS Test Completed
CP CMM	Done	Initial Tests done in R25 Lab	Require testing in R1 Lab
JEM Slice	Done	Initial Tests done in R25 Lab	Require testing in R1 Lab
JEM RoI	Done	Initial Tests done in R25 Lab	Require testing in R1 Lab
JEM CMM	no spec yet		
Energy CMM	no spec yet		

  - Two Modules tested
  - Six others to be tested soon
    - **Neil Falconer from the ESS group helping now**

Progress/Status January 2003

- **CMM (tested with DSS, GIO, RTM, TTC, CPM emulator)**
  - VME access
  - Real-time path
  - Readout data checked with the DSS and the ROD
  - Connections to/from:
    - Backplane, RTM, Front panel (CTP)
  - Tested with TTCrx dec non rad-hard and rad-hard
  - Programme FLASH via VME
  - FPGA configured from FLASH
  - Outstanding test:
    - I2C interface to the TTCrx Decoder card
  - Schematics are updated and in DO for layout

Progress/Status January 2003

- **TCM**
  - Six modules manufactured
  - Three are in use in the UK
  - One in Heidelberg
  - Need firmware updates on five (VME Display)

- **VME mount module (VMM)**
  - Six modules manufactured
  - Three are in use
  - Three modules need modifications (connectors)

Progress/Status January 2003

- **TTCrx**
  - First batch (three) of non rad-hard chips works OK
  - Second batch (seven) of non-rad hard chips not working
    - On hold until new batch of rad-hard versions are tested
  - Two cards tested with the new TTCrx chips (rad-hard)
    - The subaddr lines are not connected
    - Subaadr lines are used to latch the ID on Reset
    - This function is not used (PROM used) on RODs or the DSS
    - Six boards are assembled which can be used on the RODs or DSS (will be tested next week with the new PROMs)
    - Problem corrected and batch of 30 PCB's ordered

Progress/Status January 2003

- **Test Modules**
  - DSS Modules
    - Ten modules available
    - Four in use at RAL (2), Birmingham (1) and Mainz (1)
    - Six needs checking
  - GIO card version 2
    - Design completed, out for manufacture end of this week
    - One Back-end module
      - Xilinx XC2V250-4FG256C
    - Two Front-end modules
      - SCSI connector
      - ECL, 5 single ended and 7 differential

Progress/Status January 2003

- **Test Modules (cont.)**
  - G-Link receiver cards
  - Couple of modifications to the existing cards
    - **Lemo 00 connectors**
    - **Link locked indicators**
  - Schematics not updated yet due to CAD version problems
    - **Cadence looking into it**

Progress/Status January 2003

- **Others**
  - Glink Rear Transition module for Heidelberg
    - Received specification from Paul
    - Schematic completed
    - Send it to Heidelberg for approval
  - Adaptor Link Card for the TCM
    - For the Pre-processor and final ROD crate
    - Not started yet