CPM Testing

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Readout Controller DAQ & Roi

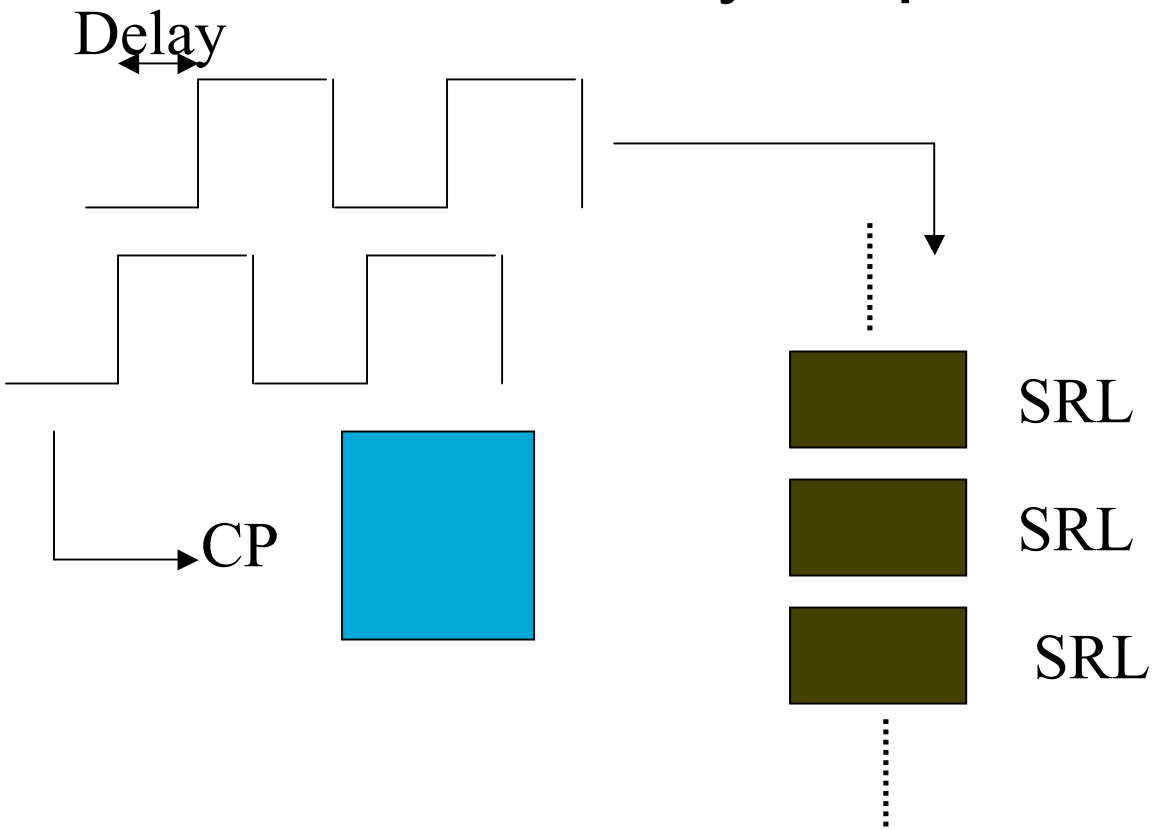
- CPM ROC Data sent to DSS with Glink Sink card:
  - On 1 L1A request: no data recovered in the DSS spy memory
  - On several L1A requests, some of them are captured: length of each packet longer by an extra word (parity data)
  - On generation of data by keeping DAV signal low: only 2/3 of memory is filled.

CP chip F/W investigations

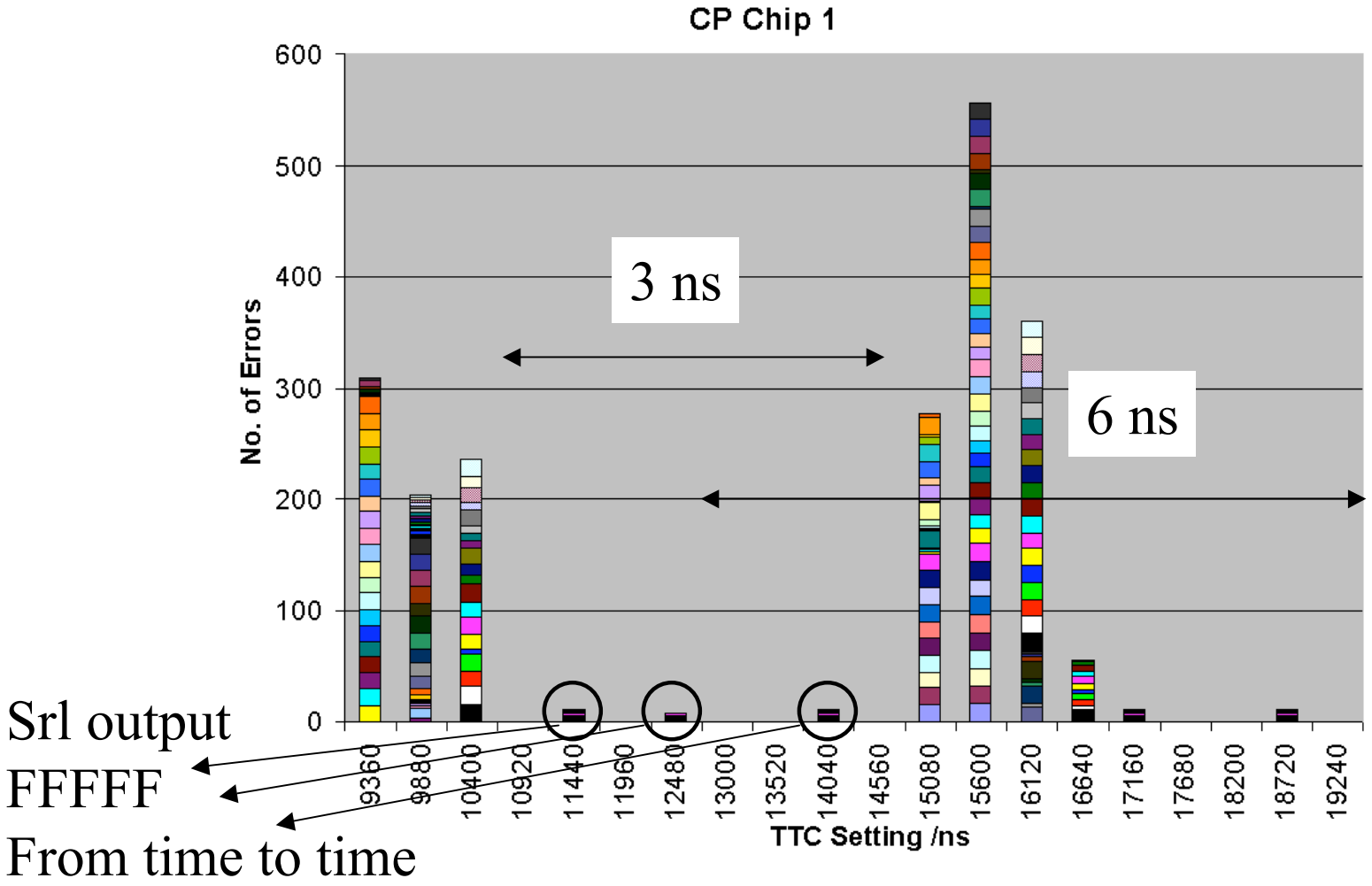
- Downloaded new F/W with 2 phases instead of 4
- With the clock between Srl and CP chip deskewed by _ tick, data are still showing wrong values, but a few less than 4 phases version (sorry! thought was working correctly earlier!)
- Generate new F/W with ONE phase now:
  - All data calibrate very well
  - Cp chip show no corrupted data !
  - Srl Chips show weird behavior now

CP Chip F/W: time window of operation

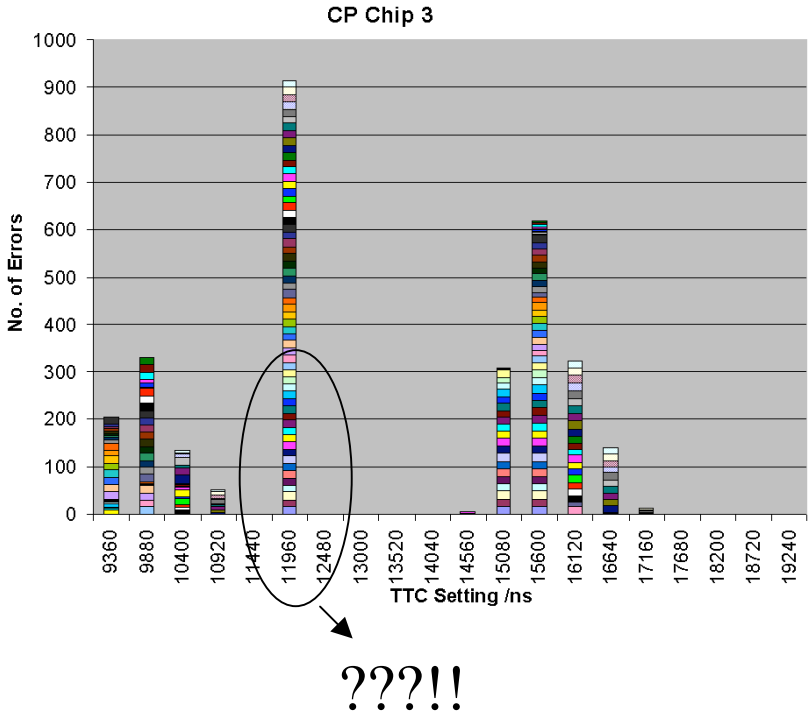
- Perform scan deskewed clock between CP and Srl by step of 104ps over 24 ns.

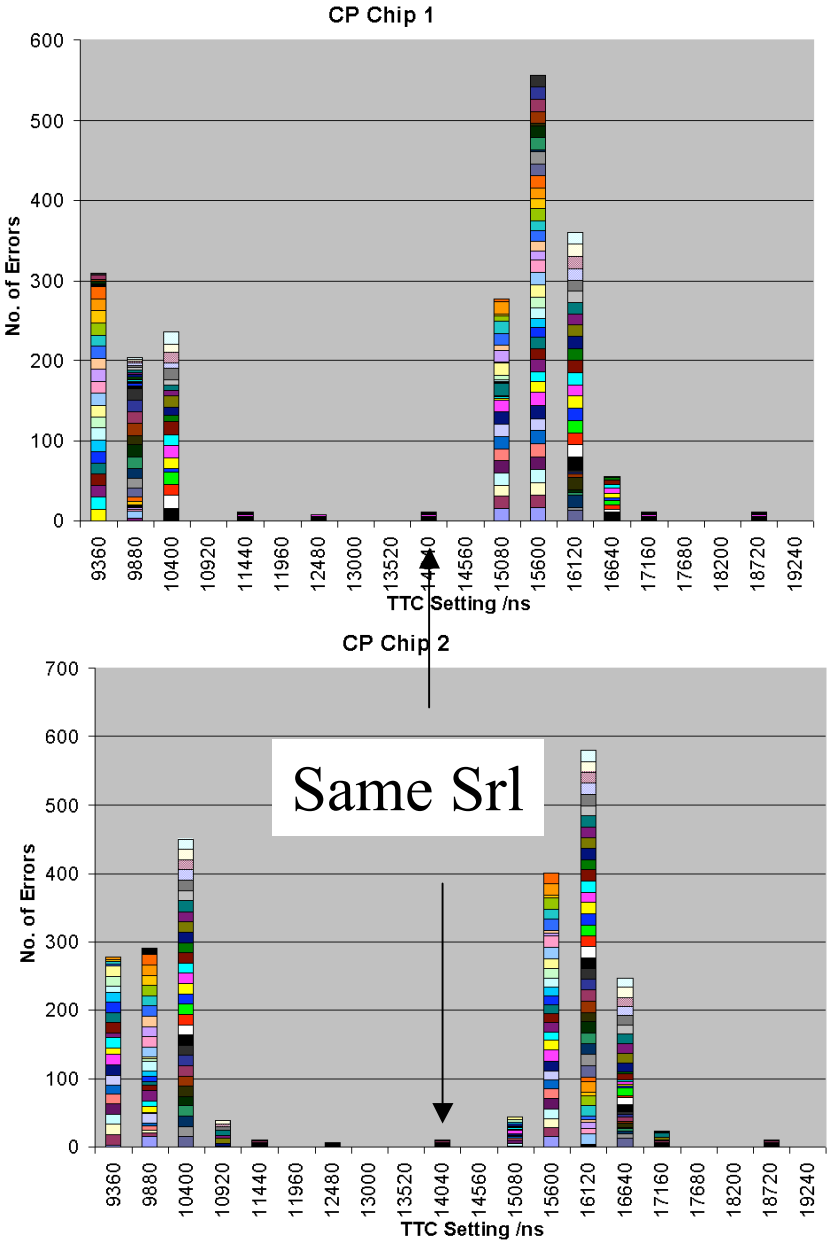


Time Window scanning – Ramp value on each input pin of Cp Chip



Chip 1, 2 and 3

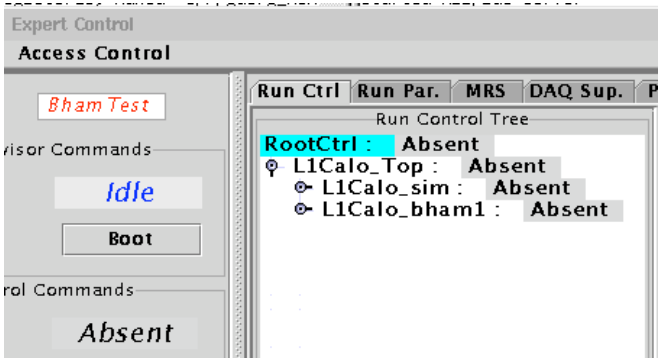

CP Chip 3
No. of Errors
TTC Setting /ns
???!!


CP Chip 1
No. of Errors
TTC Setting /ns
CP Chip 2
Same Srl
No. of Errors
TTC Setting /ns

Problems seen:

- Lost free error running behavior without knowing why:
  - S/W update?
  - All Srl channels fired? Power supply problems?
- Can not come back to an error free mode, due to the Srl not responding correctly:
  - DPR pointer not reset: data out of phase
  - F/W reloaded but nothing better
- -> new problem, need more investigation

CPM Services Integrated with Run Controller



- Lot of works done thanks to Steve, Christian, Bruce and Murrough
- Enable to make long term run with errors checking
- Plan:
  - Test Glink output similar as CP-SRL
  - More SRL-CP chip tests with scanpath configuration

Next step: soak test on Lvds Rx

- In order to perform reliable soak test on LVDS signals, 5 more DSSs are needed, to check for cross-talk between all input channels.
- Extra DSSs might required one extra crate, one CPU single board and 5 TTCdec card
  - Question: how many slots a DSS need?
  - if 2 slots required, we are ok with no extra crate but we need to remove the bit3 system: 1 extra CPU is still needed
- SRL F/W will be modified to perform only Bit Error Rate measurement

Next step: Backplane Testing – CP Algorithm

- Backplane signal testing required extra CPMs
  - 1 extra CPM will be available soon
  - 2 more could be done quickly, half populated (no CP chips), to only drive signal on backplane toward a CPM on test
  - CP Algorithm will be also fully investigated with physics data
- GIO card needed to test real time data path

Shopping list for a full B'ham CPM test bench

Material	Numbers required	Available	Extra Needed	Where	When extra needed
CPM	4	2	2	B'ham	now
DSS	6	1	5	Ral	weeks
DB LVDS Tx	10	5	5	B'ham	weeks
DB Glink Rx	1	1	0	Ral	-
GIO card	1	0	1	Ral	now
CMM emulator	1	1	0	B'ham	-
6U crate	2	1	0 or 1		weeks
CPU	3	1	1 or 2	Concurrent	weeks
Optical fan out	2	1	1	CERN?	weeks
TTCDec card (with I2C access)	9	2	7	Ral	weeks
LVDS Cable	20	22	0	B'ham	weeks