CPM Prototype Hardware Status

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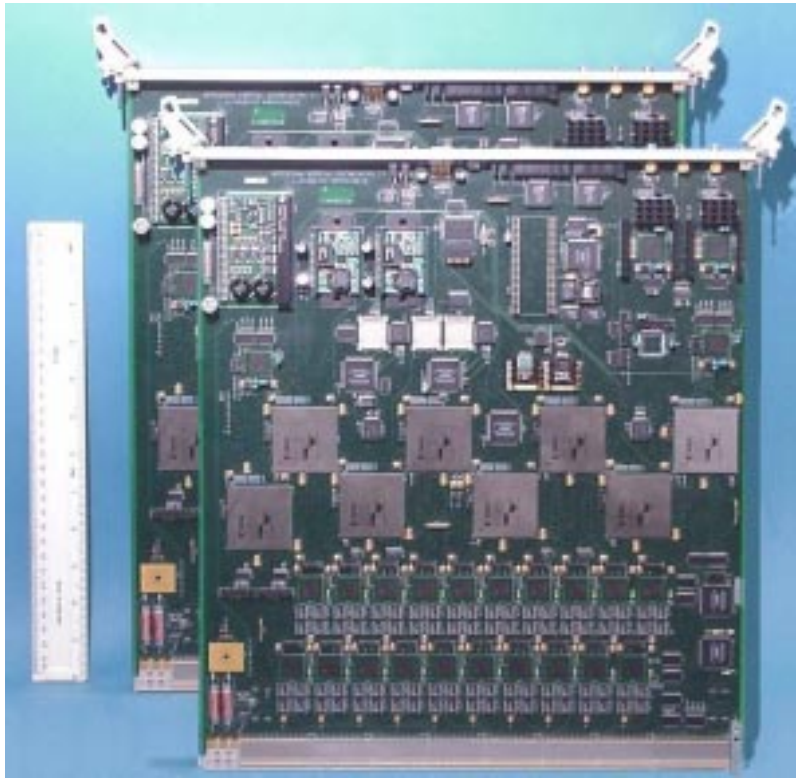
- Summary



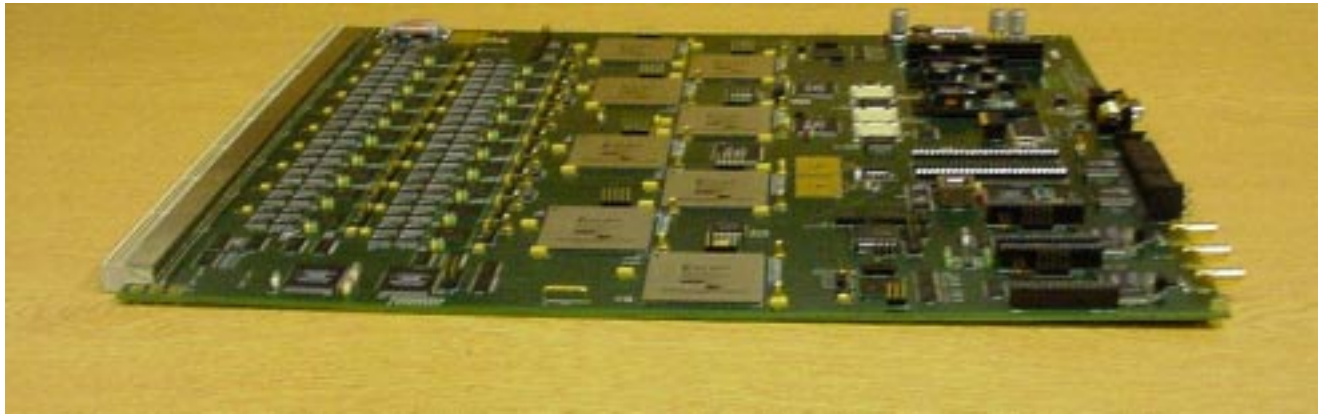
R. Staley

Hardware

Second CPM now back from Assembly.

Mechanical Assembly completed. Ready for JTAG/BS test.

But Module is warped / bowed by 3mm at centre:



Test Status (Tests done CPM #1)

- VME erase/program/read of FLASH. OK
- FPGAs configure from FLASH. (99 %)
- TTC clock distribution. OK
- Onboard 160Mb/s transmission working well.

  (but problems within CP FPGA)
- Backplane 160 Mb/s transmission suffers from reflections and attenuation. (more detail shown later)
- Glink connection from ROC to DSS working.

Test Status (Tests to do)

CPM#1 - still to complete Design Evaluation:

- Check All 80 LVDS links together
- Backplane I/O , understand signal 'distortion'
- Test Hit Sum FPGAs and output to CMM slot
- … (Gilles / Steve)

CPM#2 assembly completed, Module powers-up OK.

- Ready for JTAG/BS test. Then copy testing of CPM#1

Test Status (Tests to do)

DSS/LVDS daughter cards (new layout) :

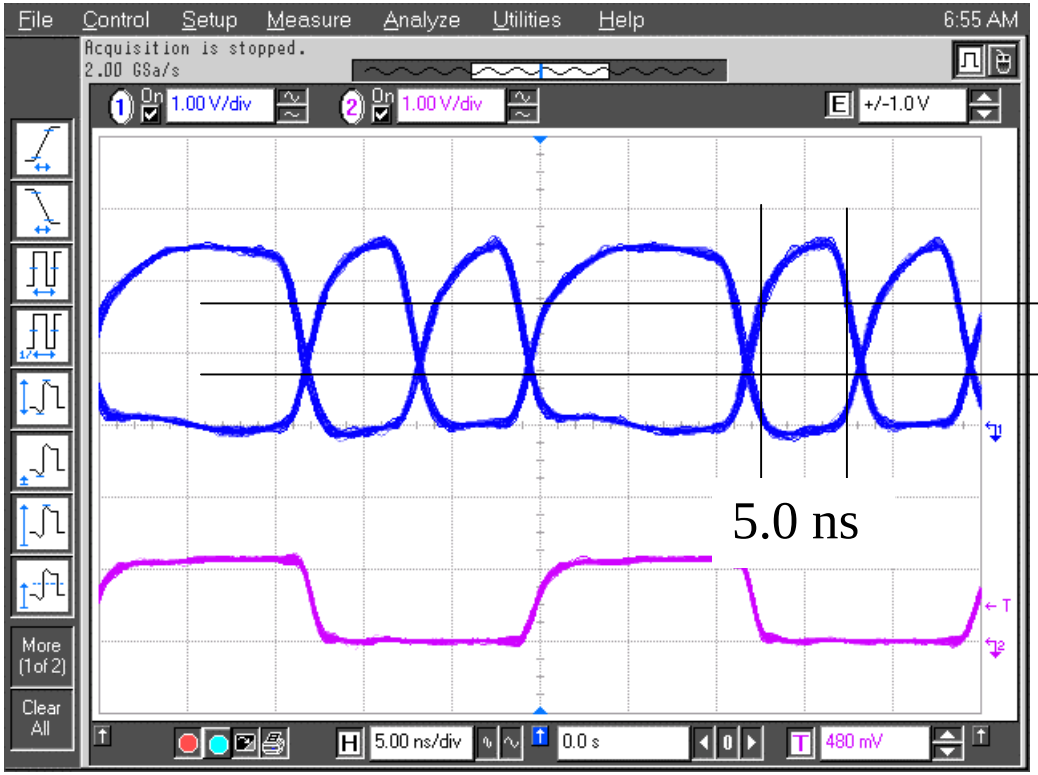
5 daughter cards assembled but untested
(EEPROM = lvds_source_6.mcs)

5 Bare PCBs.

10 daughter cards needed to drive all 80 LVDS inputs of 1 CPM.

160 Mb/s Links

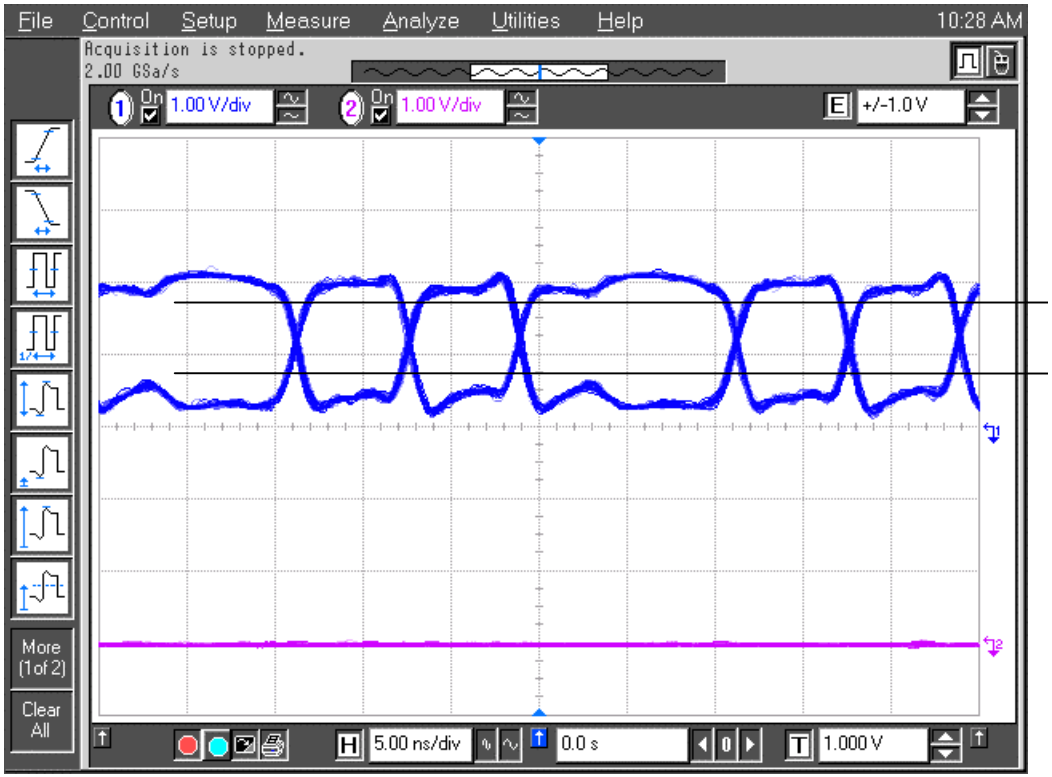
Typical CP chip input direct from Serialiser (series terminated):



1.7V V_{ih}
0.7V V_{il}
} CMOS2 thresholds

Typical CP chip input via backplane (parallel terminated):

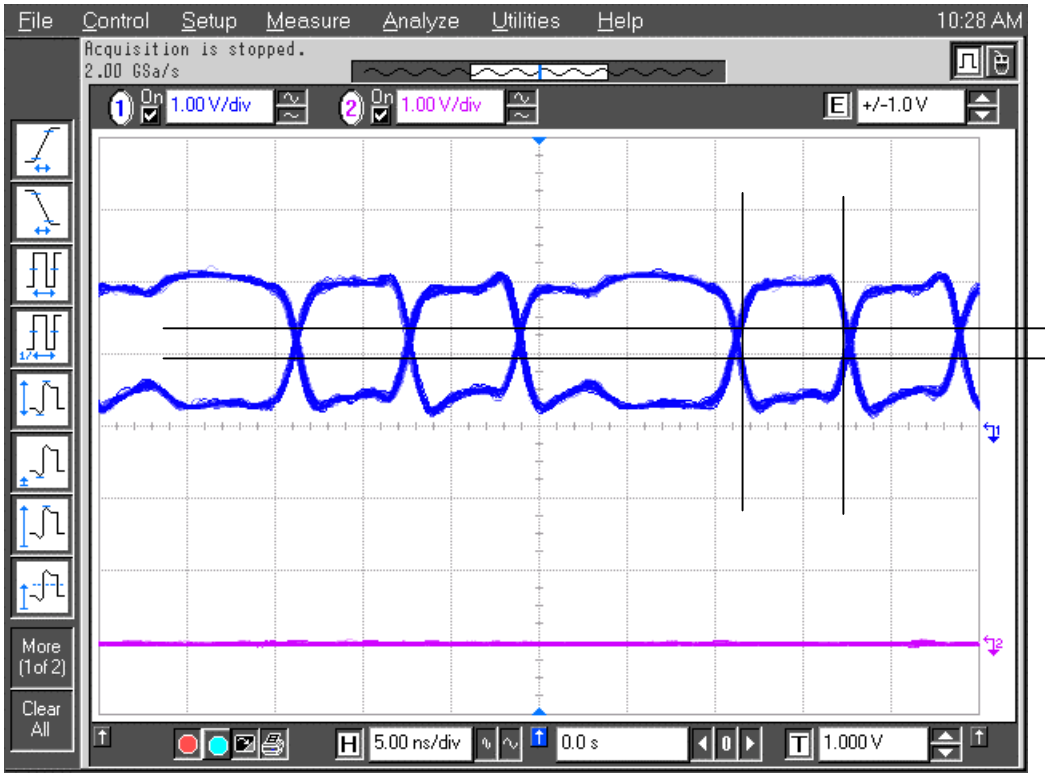
Effects of reflections and attenuation:



1.7V V_{ih} } CMOS2 thresholds

0.7V V_{il}

We need CP FPGA to be using better defined input thresholds:



V_{ref} + 0.2v
V_{ref} - 0.2v
} CTT / SSTL2

… but this scheme needs 30 Vref inputs, which are unconnected on present CPM PCB. Circuit will be included on next PCB layout.

160 Mb/s links revisited.

Why are the intra-module links different to the inter-module links on the present CPM? (Both are transmission lines)

- Intra-module links are point-to-point ,
  -can be series terminated at source.

- Incoming backplane signal directly connects 3 CP chips. (< pin count).
  - must have parallel termination at far end.

Series termination could only be used on inter-module links if extra buffers placed on receiving module to actively fan-out the signal.

Disadvantages:

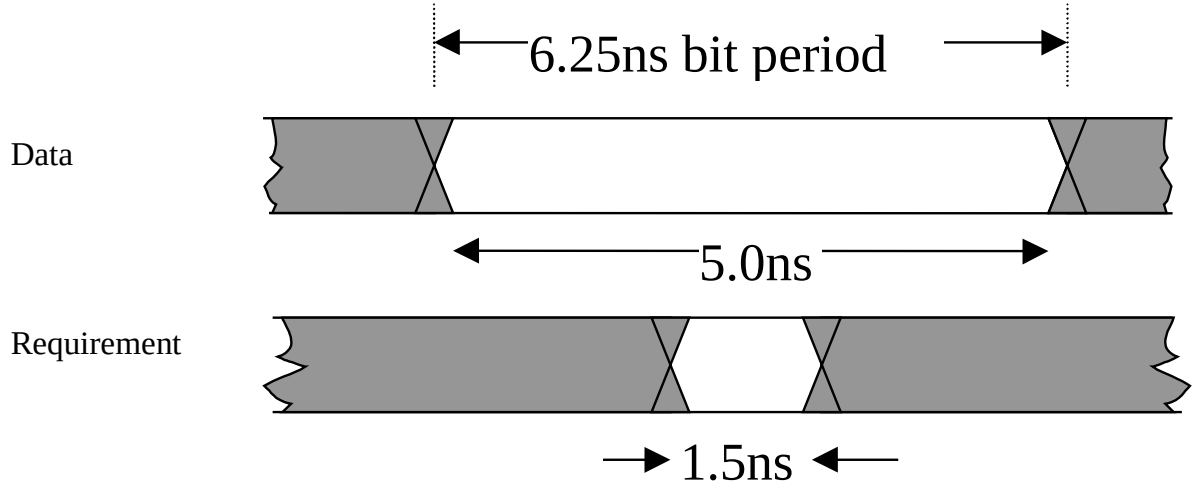
- 384 signals have to be regenerated from the 160 inputs.
  24 extra packages

- No direct connection between Serialiser and CP chip.
  What I/O standard for buffer? PCB footprint.

- More delay

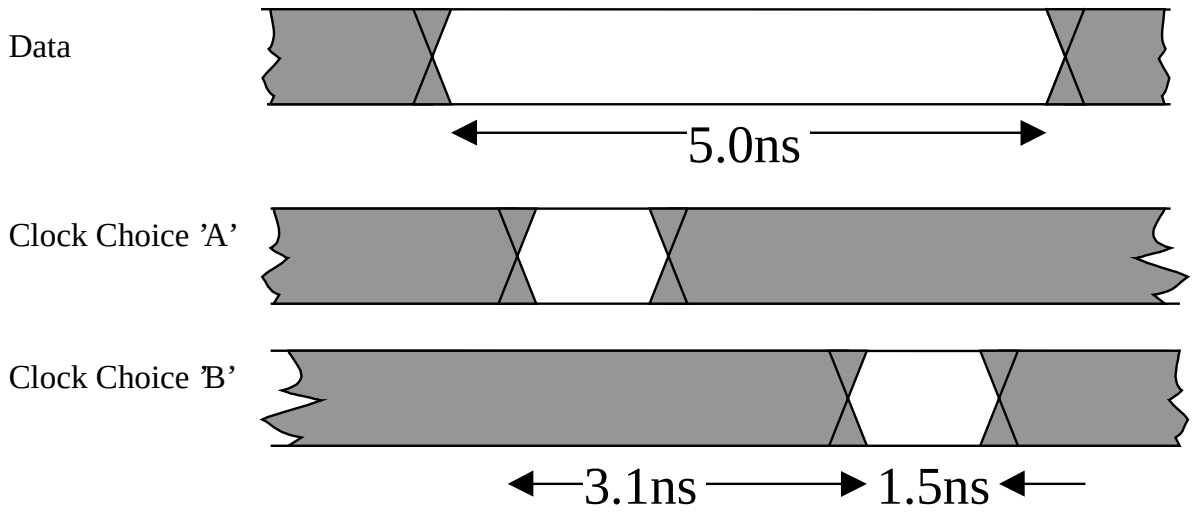
Timing margins of CP chip inputs:

Given data is stable for 5.0ns during any bit period, and VirtexE IOB or 5input CLB register has a 1.5ns set-up+hold window :



Can only adjust clock delay independently on 108 inputs of CP FPGA by selecting a limited number of clock phases to sample the data.
This is a general solution to capturing data with unknown delay, so…

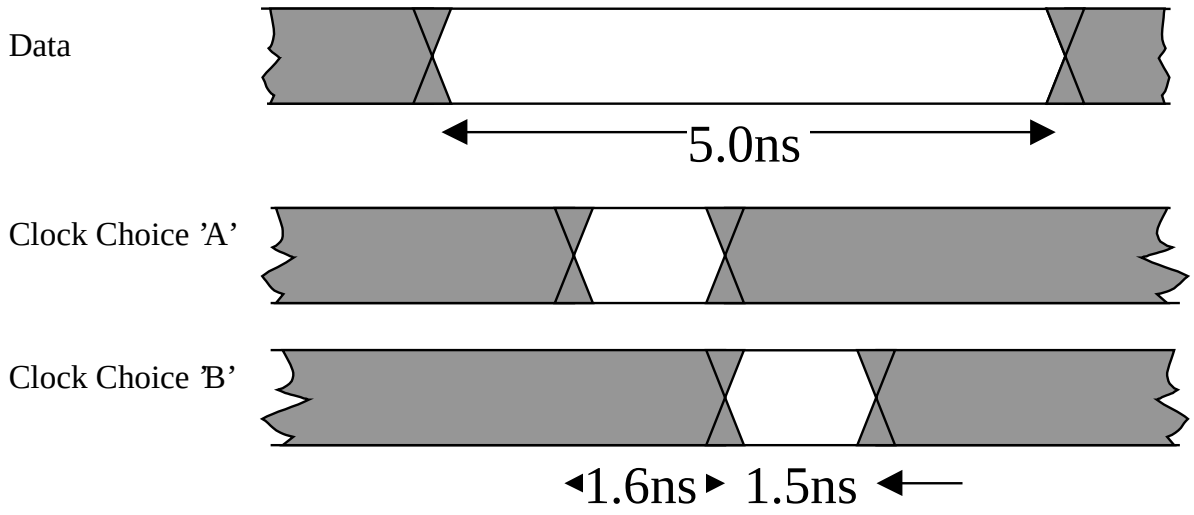
Using 2 phases (6.25ns ÷ 2), either choice of phase could lie very close to transition (to reduce routing problems within CP chip):



S+H window within 0.2ns of transition.

(5.0 - 3.1 - 1.5) / 2

Using 4 phases (6.25ns ÷ 4), the timing margins originally proposed:



S+H window within 1.0ns of transition.

(5.0 - 1.5 - 1.5) / 2

Power Supplies

Powering-on 9U crate sometimes disrupts nearby CPU crates.
At Birmingham , the CPU crate is reset.

Both 5V and 3.3V PSUs specified with a turn-on surge of ~ 35A.

Fitting additional filter has helped, but still 1 in 10.

Propose delaying the turn-on of 3.3V, until after 5V PSU stable.

One 70A pulse replaced by two 35A pulses.

Further Assembly

CPM#3 & 4 - without CP FPGAs.

Allow Backplane I/O to be fully tested at Birmingham

Summary

Making steady progress with testing. No Show-stoppers yet, but:

- Problems with capture of 160Mb/s data inside CP FPGA. (reducing calibration to 2 phases - iffy)
- Quality of inter-module links must be improved.
- Mechanical problems - warping , bending on insertion
- CPM #2 assembled. JTAG/BS test soon.