JEM Status and Test Results

- Hardware status JEM0
- Hardware status JEM1
- RAL test results

JEM**0** Status

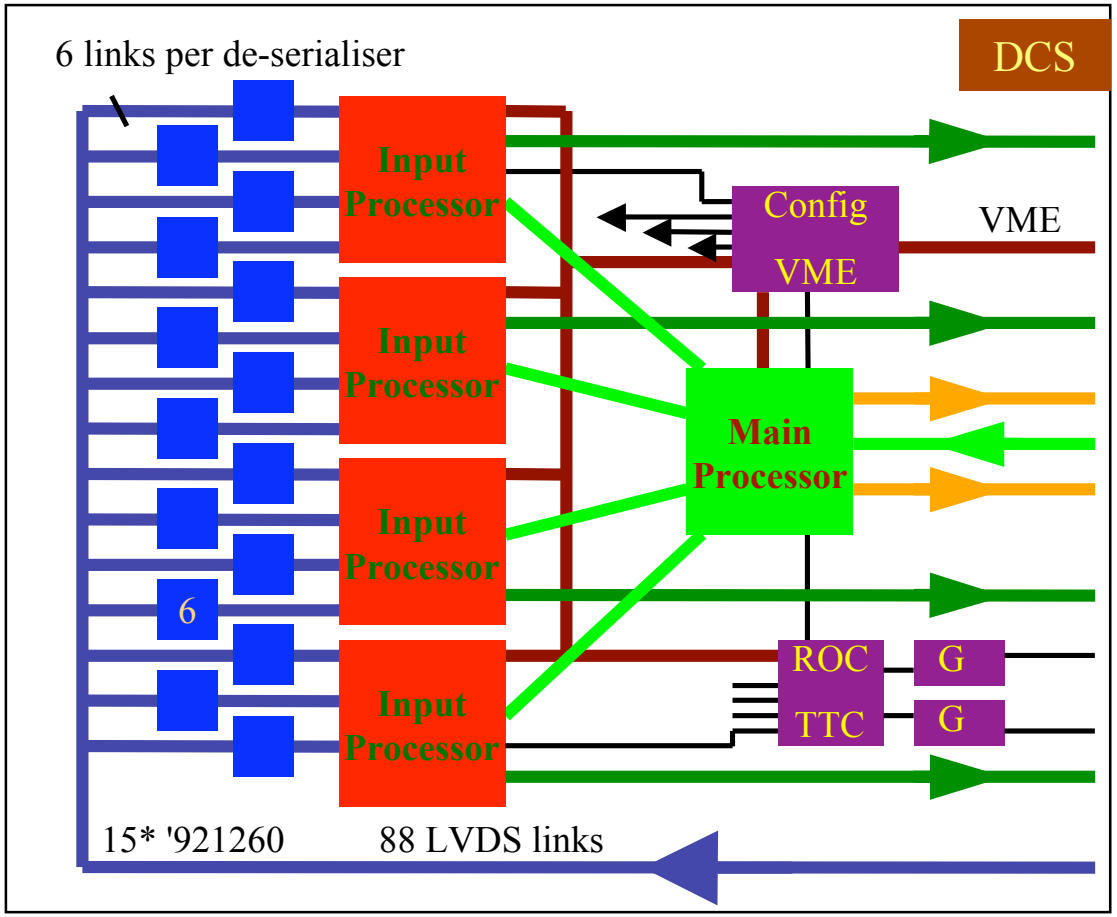
- 3 **JEM0**s up and running:
  - JEM0.0 used for standalone tests only (Mainz)
  - JEM0.1 fully qualified module0
  - JEM0.2 (like JEM0.1 but main=XCV1600E)
- JEM0.1 and JEM0.2 under test at RAL (OK)
- Hardware fully assembled and tested, apart from CAN and flash configurator.
- Firmware near-final
- Continue to improve HDL code (Andrea)
- Jet code speed problem resolved (45 MHz)
- 2nd deskewed clock for FIO links to be introduced
- ROI R/S code needs to be modified
- Tests on integrated jet code and ROI required

JEM1 block diagram

15 x 6-channel de-serialisers : SCAN921260

4 Input Processors : XC2V1500

Main Processor XC2V2000



JEM1 : Re-design

JEM1 : increased routing density due to new packages used on FPGAs (Virtex-II) and de-serialisers. Xilinx reference layout not applicable to large and thick PCBs due to requirements on precision of via position.

→ Use daughter modules on JEM1 for

- Input stage (de-serialiser and input processor)
- TTC
- ROC

Mini-review at RAL in December, 2002

Bruno currently working on input module

List of Modifications JEM0 → JEM1

- Replace de-serialisers by compatible 6-channel devices with B/Scan facility. (Allow for use of redundant channel to reduce the need for re-work of the de-serialiser BGAs)
- Replace 11 input FPGAs (8-channels each) by 4 Virtex-II chips
- Reduce board routing complexity and improve serviceability by using input daughter modules (24 channels each)
- Make input FPGA control path (VME) compatible to the one used on JEM0.0 main processor (point-to-point, no ring bus)
- Widen on-board VME control paths slightly
- Replace main processor by larger Virtex II in 1.27mm BGA package
- Use 1.5V signalling where possible (previously 2.5V)

List of Modifications JEM0 → JEM1 (2)

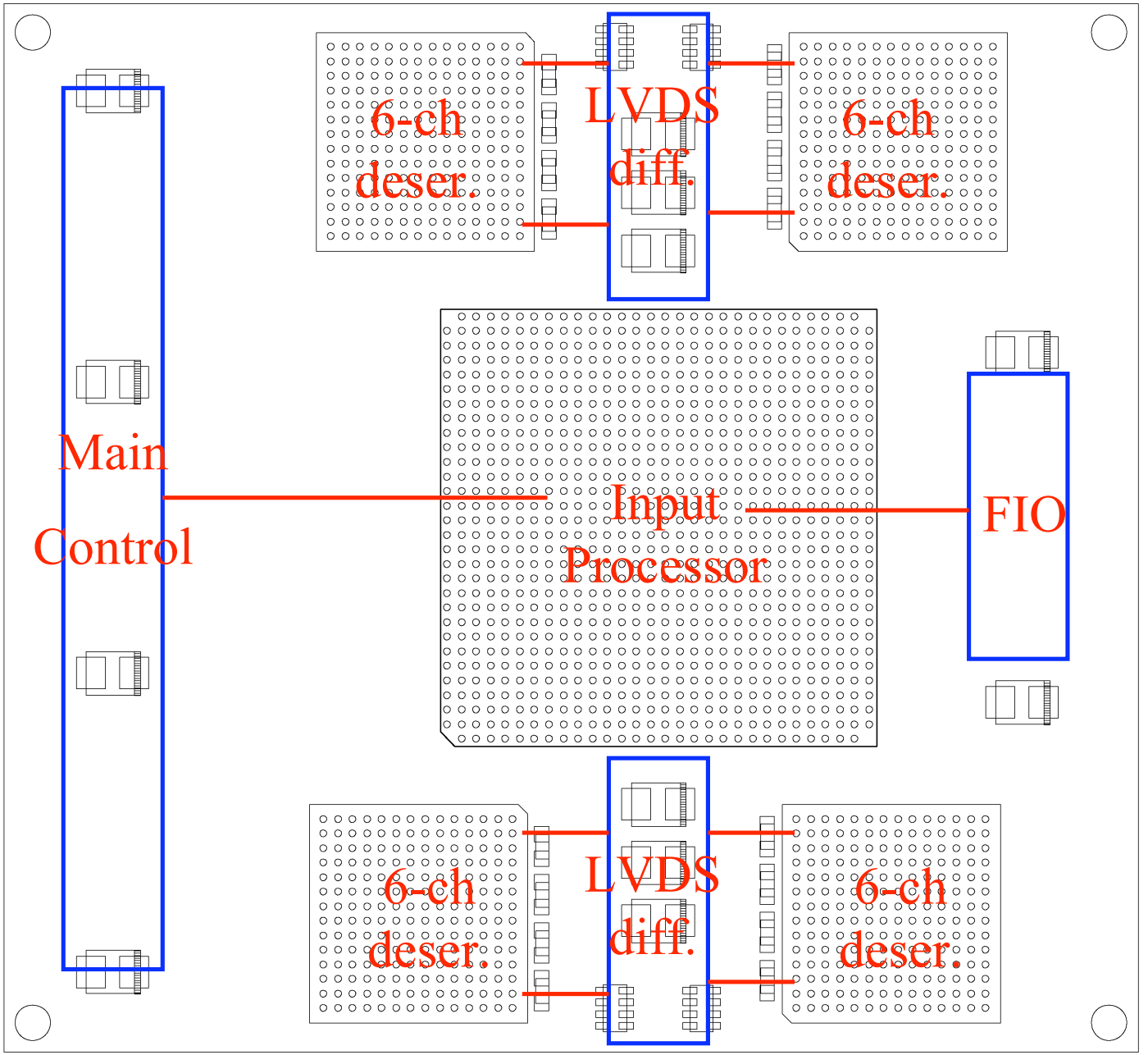
- Use internal source termination (DCI) on all signals (was discrete source termination on JEM0)
- Provide the ROC with full access to TTCrx chip
- Widen TTC/DAQ paths to the processors slightly
- Move TTC control and clock mirror into ROC
- Replace all CPLDs by a single FPGA configured from flash memory
- Add parallel flash memory for processor configuration (similar to CP)
- Make CAN H/W identical to CP (Fujitsu)

Input Module
top view

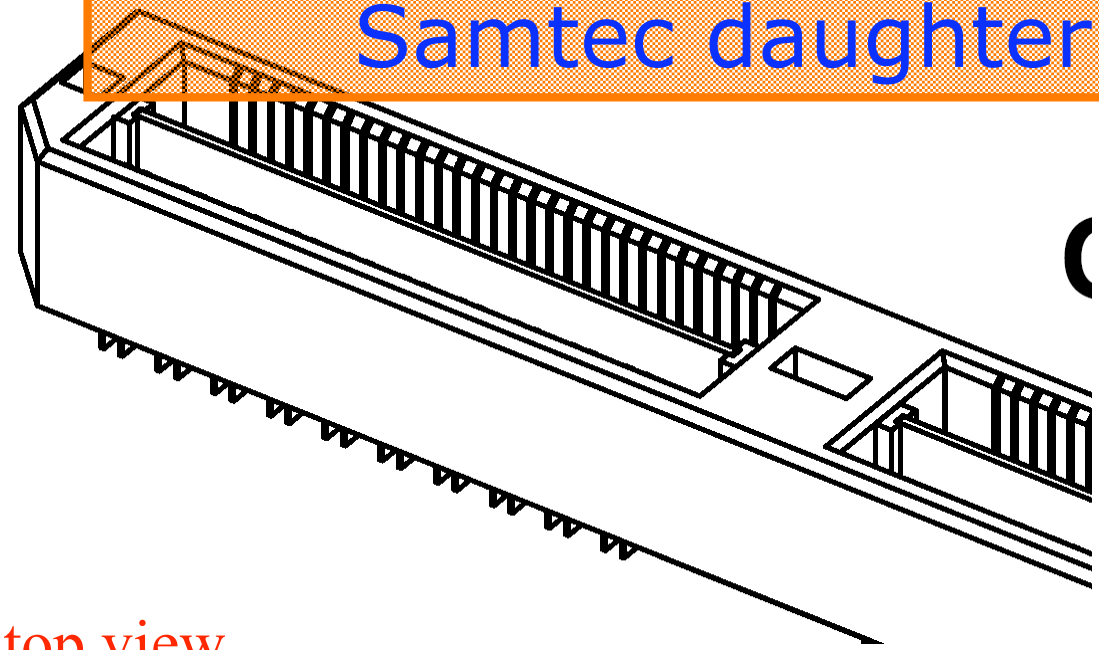
Connector
(Bottom)

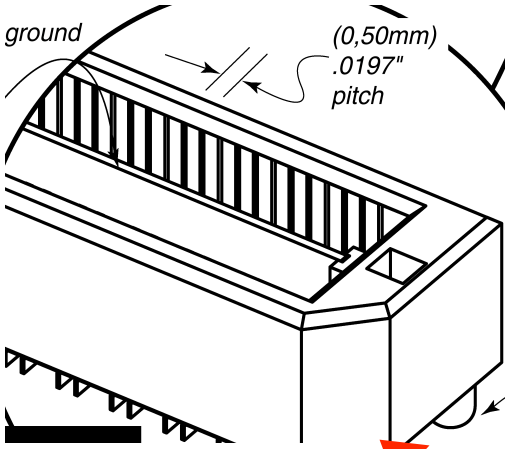
Module size:
72x78mm

100R differential
connectors
for LVDS

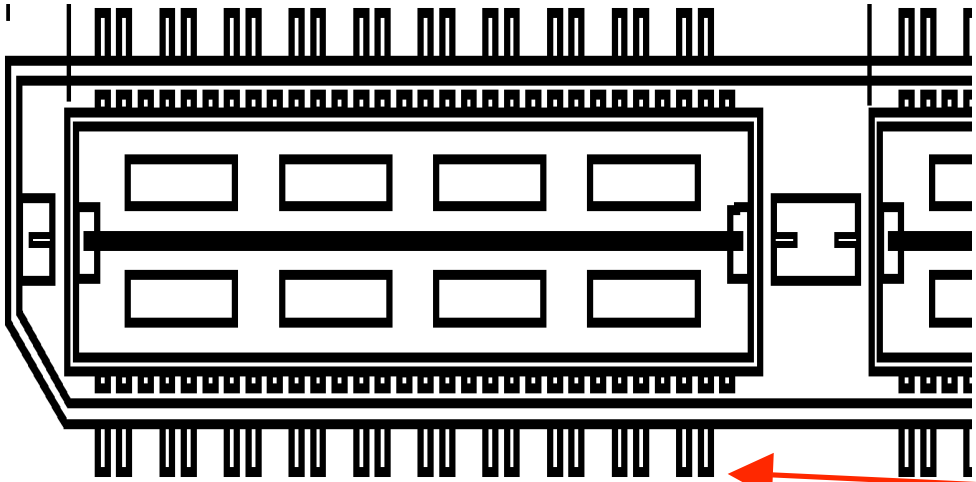


Samtec daughter connectors





top view



alignment pin

differential pairs

differential impedance:
100.0 to 89.4@ 250pS
100.0 to 95.0@ 500pS

JEM1 status

- Daughter connectors:
  samples available, look v. good
- Input module:
  layout under way
- Main board:
  capture not yet started
- TTC/ROC daughter:
  details to be decided on

RAL Tests

Repeat standalone tests already done in Mainz:

- JEMs operated in a crate with local crystal clocks **ok**
- JEMs operated in a crate with a CPU and a TCM (ok)
- JEM0.1 broken during tests (VME access) -- repaired
- Backplane pins damaged – (repaired)
- Currently both JEMs are well and lock successfully to LVDS signals from a DSS if the **TTC signal distribution is bypassed** and the DSS is driven directly off an ECL clock generated by the TTCvi. **TTC jitter !**

Next steps:

- Test input synchronisation and input delay control (S/W)
- Test FIO links (S/W, F/W)
- **Further tests on jitter tolerance required**