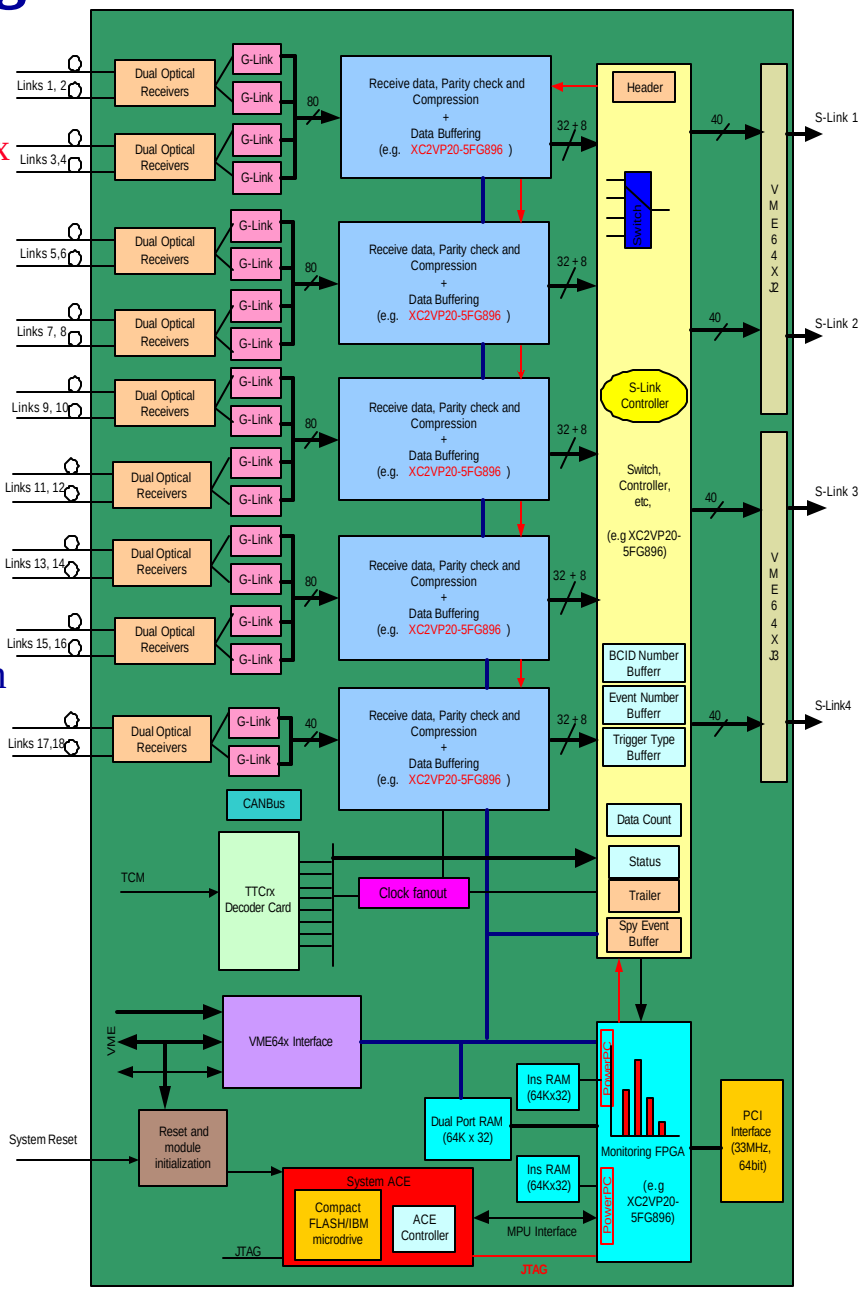
9U ROD

- 9U ROD for ATLAS First Level Trigger Processor
- Specification was reviewed on the 1st of July 03
- ROD Requirements
  - **Collect data from several modules**
    - **Pre-processor**
    - **JEM**
    - **CPM**
    - **CMM**
  - **RoI as well as DAQ data**
  - **Error detection**
  - **Data compression**
  - **Format event data**
  - **Interface to the readout links (S-link)**
  - **Monitoring S-Link data (spy)**
  - **Receive TTC signals**
  - **Interface to CTP (ROD Busy)**
  - **Operate at level-1 event rate**
  - **CANBus for monitoring module temperature, voltages, etc**

9U ROD

• Block Diagram of 9U ROD

- 18 x Inputs
  - Dual Optical Rx
  - G-links
- Input FPGA
- Switch FPGA
- S-Link Interface
- Monitor FPGA
- VME FPGA
- Module Initialisation
- TTC Interface
- System ACE (CF)



9U ROD

- **'Input FPGA'**
  - Receive G-Link Data (four G-Links)
  - Parity Check
  - Compression
  - Data Buffering
  - XC2VP20-5FF896
    - 556 I/O
    - 1,584 Kb Block RAM
    - ~11K deep x 32 bits per input

- **'Switch FPGA'**
  - Interface between the Input FPGA and S-links
  - XC2VP20-5FF896
    - ~11K deep x 32 Bits per S-link (4)
    - Four high-speed links to 'Monitor FPGA'

9U ROD

- **'Monitor FPGA'**
  - **'Process' spy data**
  - **XC2VP20-5FF896**
    - **Four high-speed (Rocket I/O) links to 'Switch FPGA'**
      - **To be used if all four spy buffers need to be copied simultaneously**
  - **Two Power PCs available**
    - **Interface to Instruction RAM**
  - **Interface to Dual port RAM**
  - **PCI interface for PMC cards**
  - **VME interface to Spy buffers**

- **'VME FPGA'**
  - **VME 64x interface**

- **Module Initialisation CPLD**
  - **Initialisation and Reset functions**

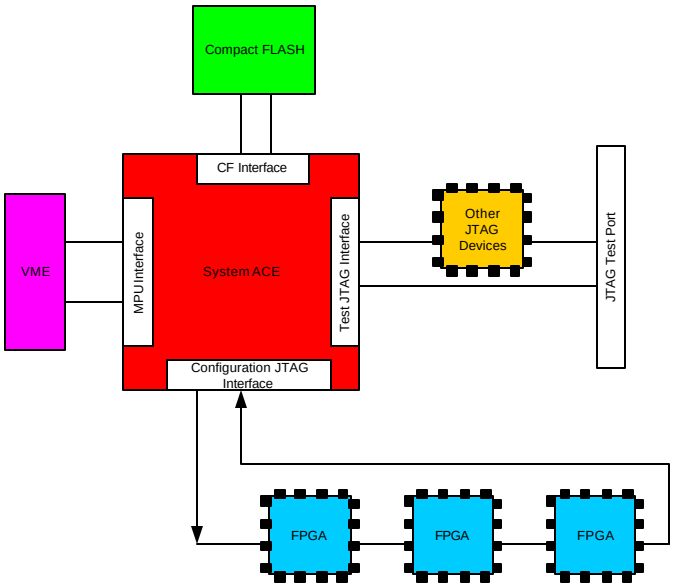
9U ROD

- **Firmware**
  - **10 Variants**
  - 1 Pre-processor Slice
  - 2 CP Slice
  - 3 CP RoI
  - 4 JEM Slice
  - 5 JEM RoI
  - 6 CMM-CP slice
  - 7 CMM-JEM slice
  - 8 CMM-JEM RoI
  - 9 CMM-Energy slice
  - 10 CMM-Energy RoI

  - **5 'collections' for configuration**
- **E.g. 'Collection 1' - CPRoI**
  - **Input FPGAs 1-4 CPM RoI firmware**
  - **Input FPGA 5 CMM RoI firmware**
- **Five configurations (+ test configurations) resident on ROD**

9U ROD

- **System ACE (CF)**
  - **All configurations held in CF**
  - **Configured via JTAG**
  - **Select appropriate collection (8 max) by:**
    - **VME register (module initialisation)**
    - **Module code**
      - **e.g Geographical Address**



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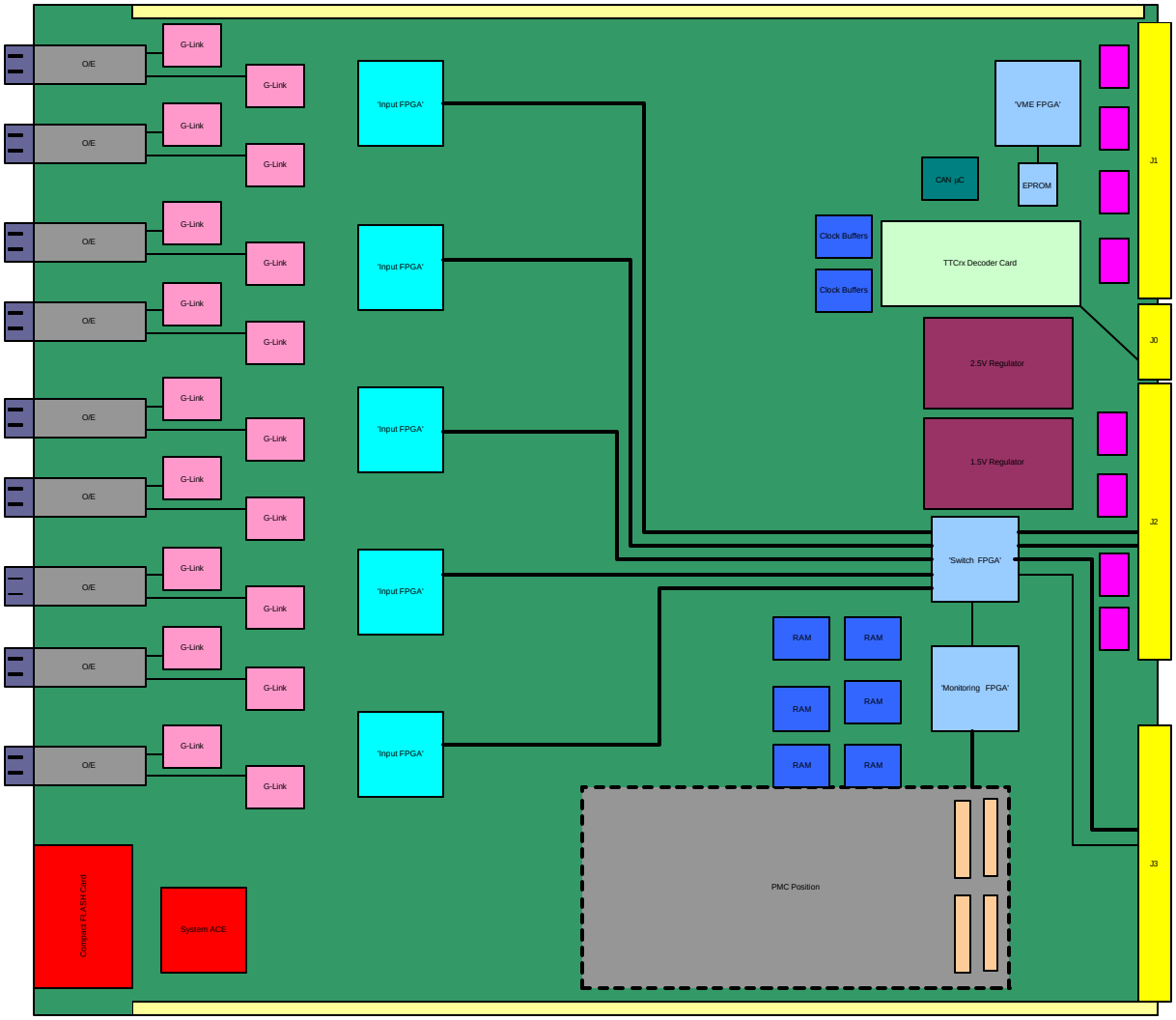
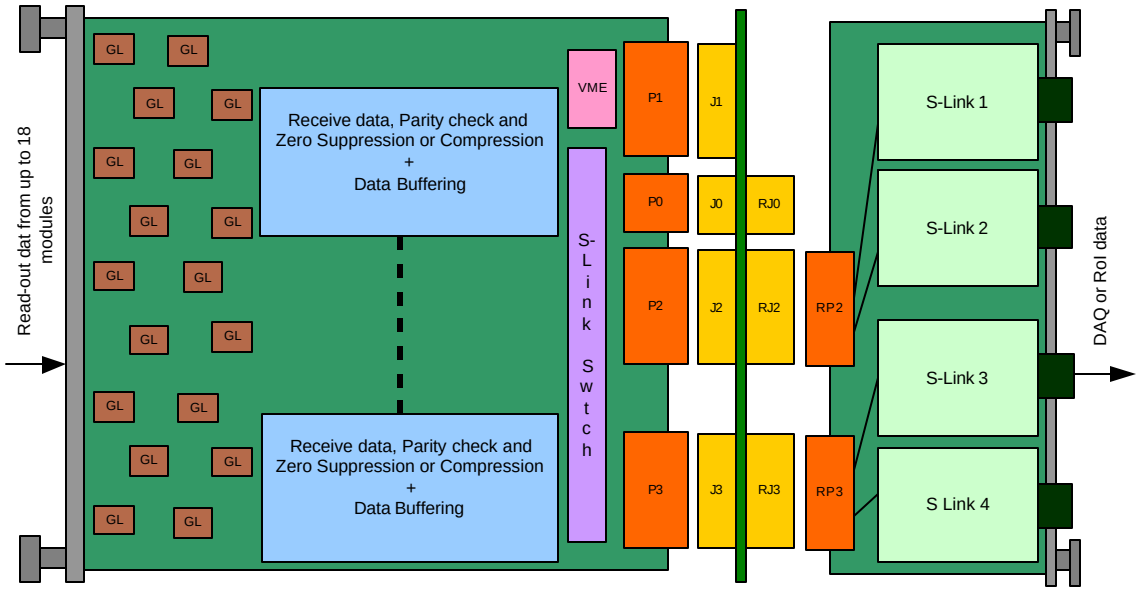
Floor plan (Provisional)



9U ROD

- **ROD to S-Link**
  - **Four S-Links on VME rear transition module**
    - **RAL to design, based on CERN S2VME64x Design**
  - **S-Link selectable from Switch FPGA**



9U ROD

- **Design Team**
  - Ian, James and Panagiotis

- **Time Scales**
  - Module available in Q?, 2004
    - PDR held on 1st July 2003
    - Sorting out actions from PDR
    - Urgently need to sign-off
      - FPGA designs (3 months)
      - Complete schematic capture (1 month)
      - IDR and corrections! (1week)
      - Layout (1.5 months)
      - PCB manufacture (two weeks)
      - Assembly (one week)
      - Test