# CMM Status Report

- Nomenclature
- Status of CMMs 0-5
- Status of firmware
- Responsibility for CMM types
- Summary & Plans for near future

# Nomenclature

CMM #0:

- Version 1.0 design: bug prevents automatic configuration on power up.
- Lives in Heavy Duty Lab; no plans to use in slice tests.
- Used to be called CMM #1.

CMM #1-5

- Version 1.1 design: automatically configure on power up.
- Available for use in subsystem tests.
- CMM #1 used to be called CMM #6.

# Results of testing CMM 1-5

- CMM 1:
  - bad BGA joints for I2C_RST and FLC_DATA(5,7) (flash data bus)
  - intermittent problems with LVDS transceivers.
- CMM 2:
  - intermittent problems with LVDS transceivers.
- CMM 3:
  - bad BGA joint for I2C_RST,
- CMM 4:
  - no known problems
- CMM 5:
  - intermittent problems with LVDS transceivers.

- LVDS transceiver problems:
  - probably due to faulty devices
  - total of four replaced
  - problems not recurred, yet.

- BGA problems:
  - found by boundary scan, confirmed by optical inspection (ERSAscope),
  - can be worked around.

- After inspection CMM 1 displayed worse problem: no response from CPLD JTAG chain. Gone for re-assembly.

# CMM 0-6 Status

| | CMM 0 | CMM 1 | CMM 2 | CMM 3 | CMM 4 | CMM 5 |
|---|---|---|---|---|---|---|
| **location** | HDL | re-assembly | HDL | B'ham | Lab 12 | HDL |
| **CRT f/w** | n/a | none | cpcrt_vc_03<br>cpcrt_vs_08 | cpcrt_vc_00<br>cpcrt_vs_05 | cpcrt_vc_03<br>cpcrt_vs_08 | cpcrt_vc_03<br>cpcrt_vs_08 |
| **SYS f/w** | n/a | none | cpsys_04 | cpsys_04 | cpsys_04 | cpsys_04 |
| **I2C f/w** | i2c_ttc_01 | i2c_ttc_03 | i2c_ttc_03 | i2c_ttc_02 | i2c_ttc_03 | i2c_ttc_03 |
| **VME f/w** | unknown | vme_interface_2_1_2 | vme_interface_2_3 | vme_interface_2_1 | vme_interface_2_3 | vme_interface_2_3 |
| **Flash f/w** | n/a | none | FPGAloader_v2_1 | unknown | FPGAloader_v2_1 | FPGAloader_v2_1 |
| **TTC I2C ID set?** | n/a | yes | yes | unknown | yes | yes |
| **1.8v LED working?** | n/a | yes | unknown | unknown | no | no |
| **G-Link fixed?** | no | no | no | no | no | no |
| | | | | | | |

# CMM Firmware Status

- CP hit counting:
  - designed by Ian Brawn,
  - fully tested in simulation and stand-alone hardware,
  - expect change requests to keep arising from tests with DAQ.

- Jet hit counting:
  - being developed by Sam Silverstein from CP f/ware.

- Jet Energy Summing:
  - real-time algorithm block designed by Andrea Dahlhoff,
  - readout block designed and integrated by Ian.
  - readout block fully simulated (but don't yet have unified test bench for readout and real-time paths),
  - ready to be used in subsystem tests.

# Responsibility for CMM types

CP hit counting:

- wholly responsibility of RAL.

Jet hit counting:

- RAL responsible for
  - supporting all logic common to CP f/ware.
- Stockholm responsible for
  - supporting algorithm block,
  - top-level integration of design,
  - subsystem hardware tests.

Jet Energy Summing:

- RAL responsible for
  - supporting all logic except algorithm block
  - top-level integration of design.
- Mainz responsible for
  - supporting algorithm block
  - subsystem hardware tests.

- ... this is a personal interpretation of the current situation.
- Firmware support = implementing any required design changes, simulating, bug-hunting.
- All *stand-alone* testing of CMM hardware done by RAL. Other hardware tests should be planned & executed by those with the best understanding of the real-time logic; RAL to support the readout path.
- Changes to one type of CMM firmware are likely to effect others. By defining responsibility don't wish to restrict lines of communication; do wish to ensure all required work gets done (and not duplicated).

# Summary & Plans for near future

- Four CMMs have been tested and are currently in use in
  - RAL Instrumentation Lab x 2
  - RAL Trigger Lab
  - Birmingham
- Non-urgent modifications pending for all boards:
  - G-link fixes
  - firmware updates
- Plan to modify CMMs in Instrumentation Lab this week and then swap with those in trigger lab & Birmingham
- Fifth CMM available for use soon (hopefully).