CPM Prototype Hardware

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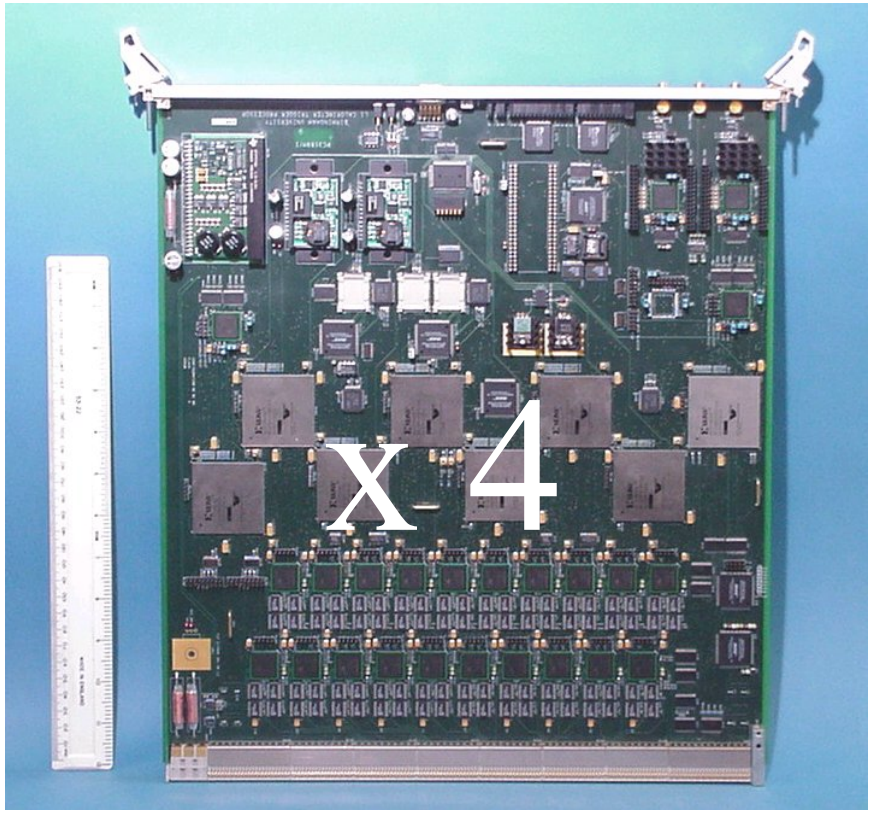


R. Staley

Hardware Status (1.0)

#1 - Assembled and fully working

#2 - Assembled, but assembly defects with 4 CP FPGAs .
Used for driving data onto backplane.

#3 - Assembled, but assembly defects with 5 Serialiser FPGAs .
Being used to test onboard CAN uC at RAL.

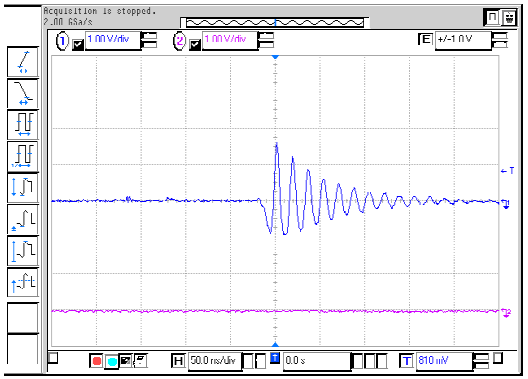
PCB Surface finish changed to Tin (as Gold / Nickel finish suspect - limited life).

#4 - Assembled and fully working.

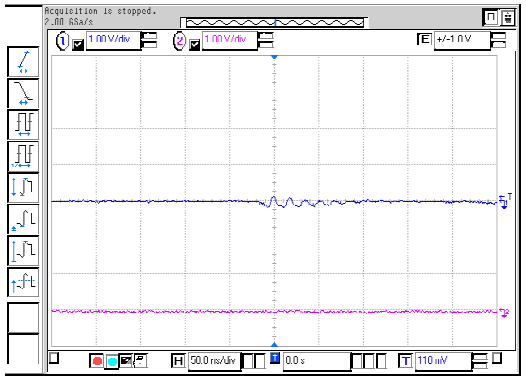
#5 - Waiting to be assembled.

Power Modules

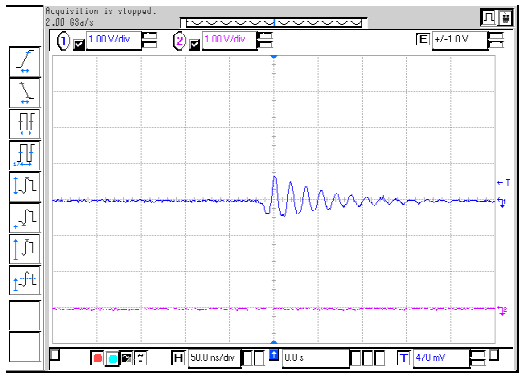
The 1.8V converter on CPM#1 failed after 1 year - V stress.
Spikes observed actually due to magnetic pick-up of scope probe:



'scope probe topside



'scope probe underside



1cm ∅ loop nearby

Cause ? Replacement fitted, and running OK > 4 months.

Next Version CPM will accept 2 different designs of Power Module.

G-Links

G-Link TXs were unstable with another CPM adjacent.

Cause: FIO termination voltage (Vtt) regulator oscillating ⇦ G-Link 5V supply (via Vtt op-amp supply).

CPM (1.0) Vtt oscillation cured. G-Link TXs OK.

CPM (1.5) Vtt different circuit, isolated from 5V.
G-Link Tx supply + extra filtering.

Next Version (1.5)

- Addition of Bracing Bars - Some Components to move
- Re-route CP backplane inputs , and check other FIO traces.
- Clock distribution. Timing must be tightly controlled. More PLLs to be added, 3 (4) clocks per CP Chip.
- New TTCdec with different connector.
- + Fibre-optic output to ROD. (Stratos module)
- CP chip to use Vref inputs. ……

Vref inputs allow reception of SSTL2 level signals.

Only minor change in Serialiser and CP FPGA firmware will be needed to move from CMOS2 to SSTL2 signal levels.

Lower switching currents -> Lower noise & power.

Better-defined thresholds -> improved timing margins.

Next version will be fully compatible with present hardware (CPM/CMM/TCM).

Existing Firmware (FPGA & CPLD) can be used on next version PCB without modification.

Timescales (1.5)

RAL Drawing Office available for CPM re-layout mid July.

- Layout Modifications should be finished Mid-End August.
- Assembled boards (assuming OK) by October.

Schematics submitted (last week) to RAL DO.
(Some Cadence Library parts need updating)

- Assembled module by XMAS ?

Summary

- Assembly problems with CPM#2 & #3 -PCB Surface Quality?
- CPM#4 with Tin plating Assembled without problems
- CPM#5 PCB also Tin plated. To be assembled.
- Work just started on re-layout of CPM (1.5)

  Aim to be debugged and tested by mid 2004.(FDR)