Cluster Processor Modules Testing: Real Time Data

Uk Meeting, Tuesday the 23th of September 2003

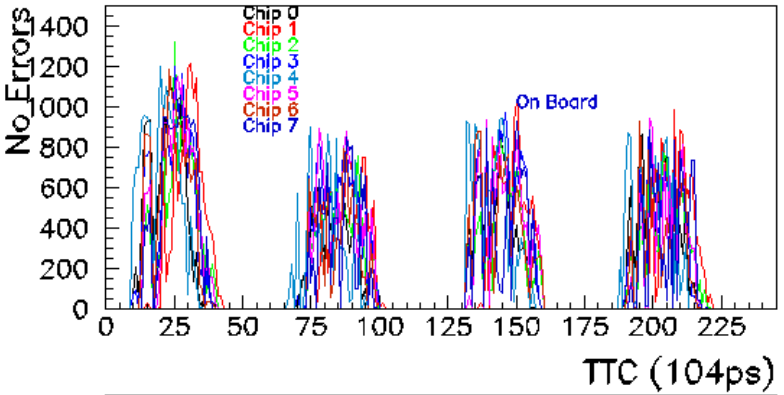
Cluster Processor Module #1.0 Ver4 has arrived

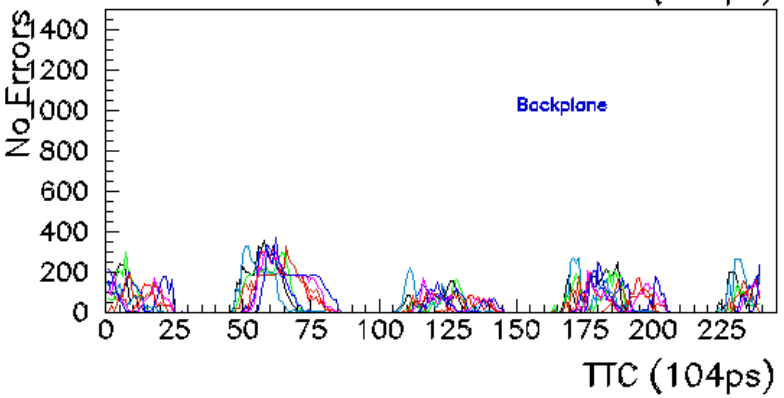
Tests and timing investigation done:

- With Scanpath mode
  - On board signal
  - Across Backplane, fan in/out left/right
- With algorithm mode
  - On RoI computed inside CP chip
  - On Hit Merged information
    - Recovered Inside DaQ RoC
    - Recovered inside CMM

CPM 1.0 Ver4: On board testing

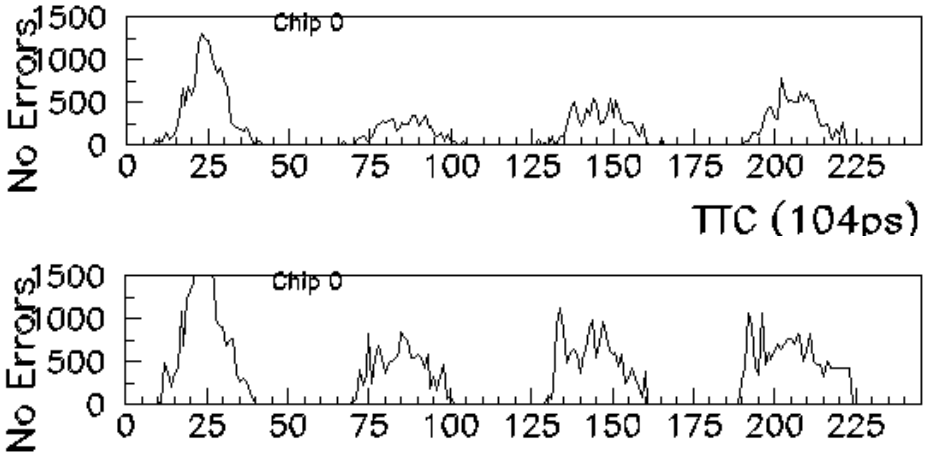
- CP chip with Scanpath mode
- Timing window better than 2.5 ns
- Used CPM#1.0 Ver2 to drive data on the backplane
- BP timing window reduced to 1.5 ns

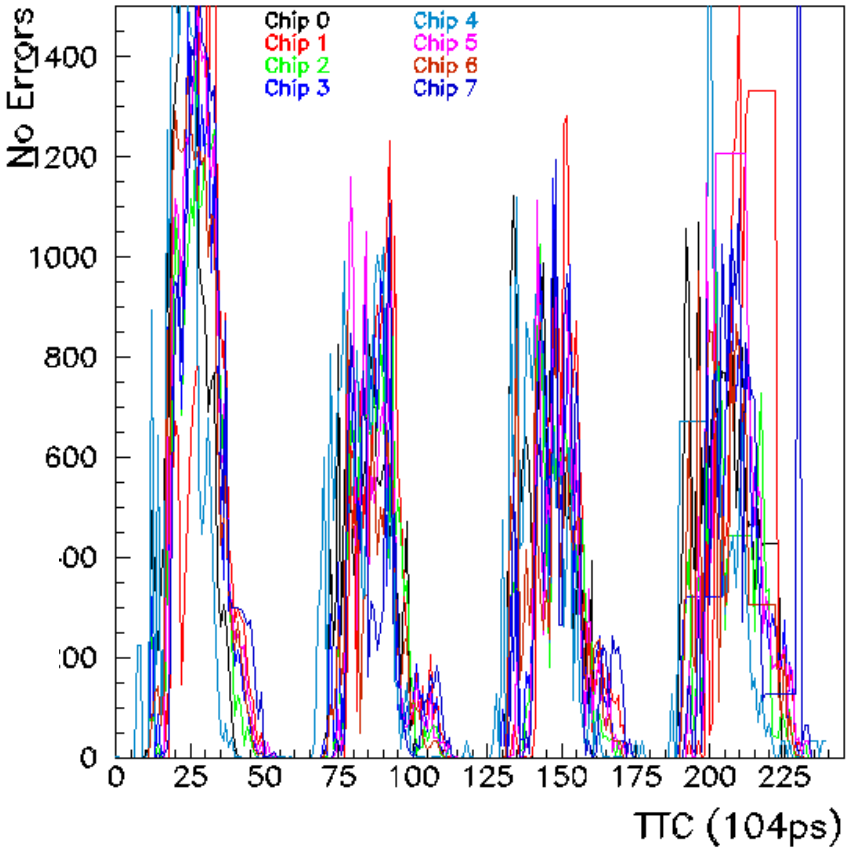




CPM1.0 Ver4 Fan in/out testing with CPM1.1

- Ver1 and Ver4 of CPM1.0 have been swapped to study fan out data
- No difference, very similar profile
- Windows reduce to less than 1 ns

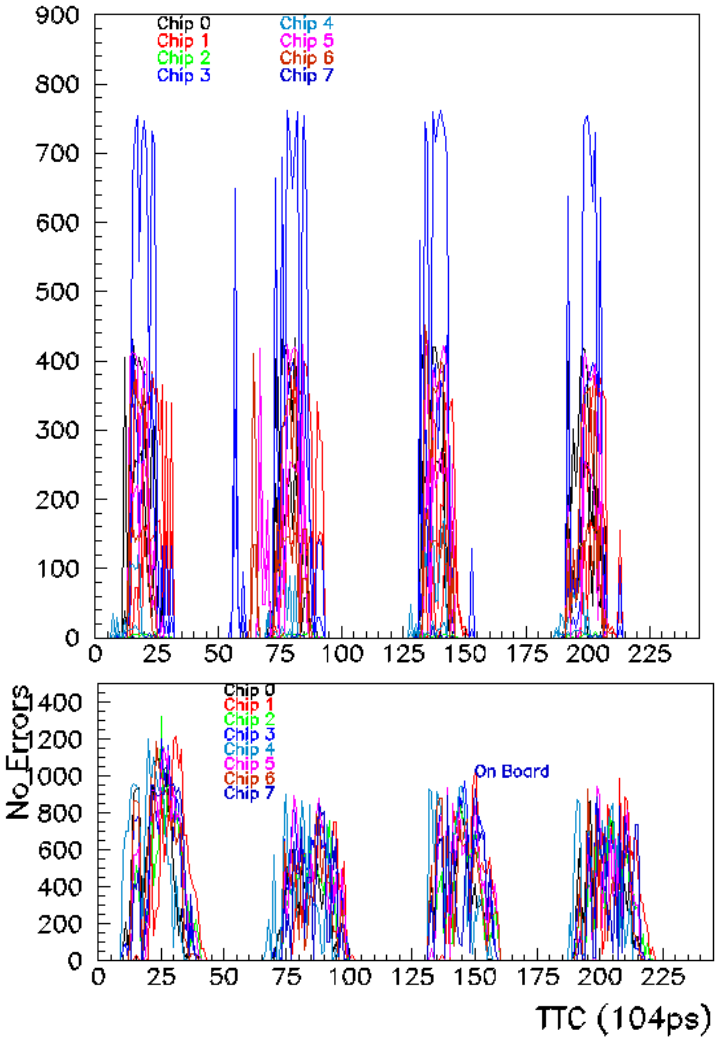




Total error , with BP, as a function of CP chip clock.

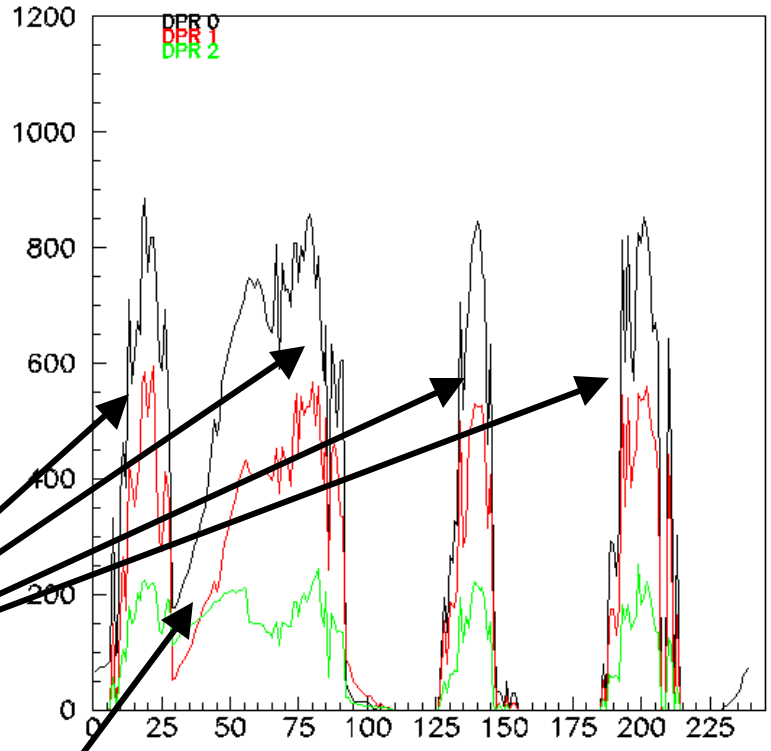
CPM#1.0: Algorithm: RoI information inside CP chip

- Timing investigation on spy memory of the CP chip with RoI information
- Algorithm timing spectrum reproduces scanpath spectrum!



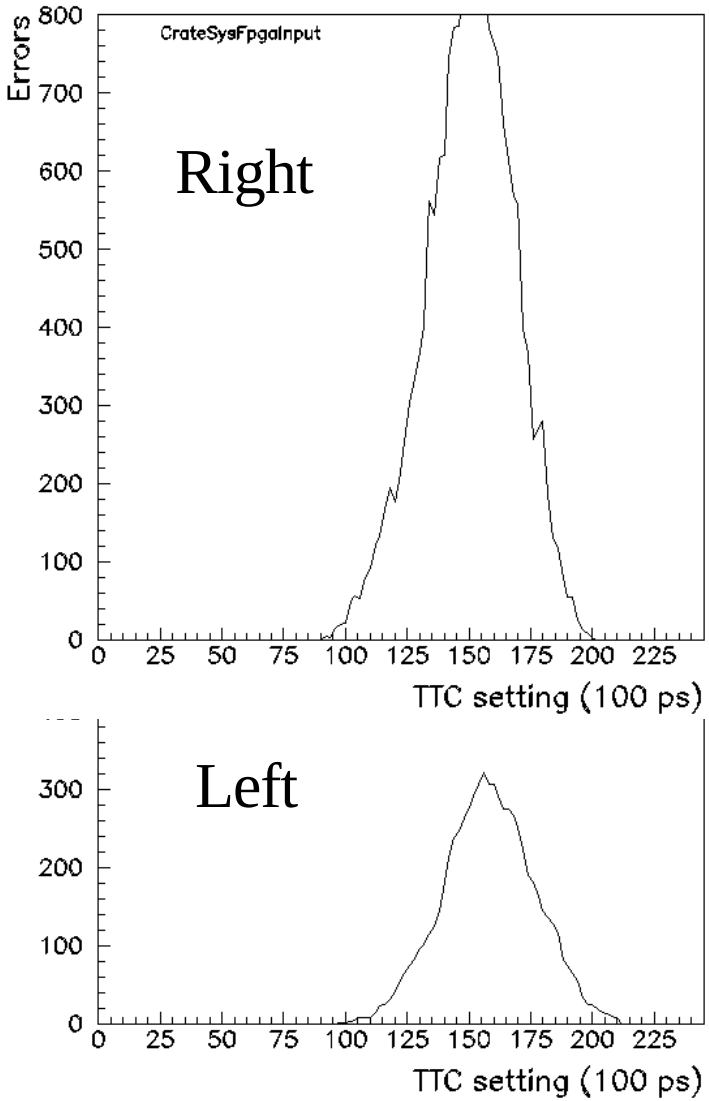
CPM#1.0: Data recovered inside spy memory of the DaQ RoC

- Timing window performed by moving CP clock (deskew2)
- Hit information sent without reclocking them at the output of the hit merger
- Timing window is a superposition:
  - CP chip timing window
  - Hit merger timing window of 12 ns, ie 40MHz period without time spent to perform all merging operation



CPM#1.0: Data sent to CMM

- Data read back inside playback memory of the CMM
- Both Cp chip and Srl Chip clocks were moved in order to keep working inside error free area of the CP chip
- CPM1.0 was in slot 12, 2 scans have been performed with CMM on right , then on left hand-side
- The difference of nº of slots is of 1, shifting the timing window by 500 ps



Next step: Crosstalk studies

- Follow Sam proposal for backplane studies
- Investigate different slots
  - Be aware the board is mechanically fragile
- BER on new CPM 1.0, Ver4, to be done
- Test on CPM1.0 Ver5 once the board is available