Test of the JEM 0.1 at RAL: Readout and Crosscheck with jemSim

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The Jet/Energy Module Prototype: JEM 0.1

Situation:

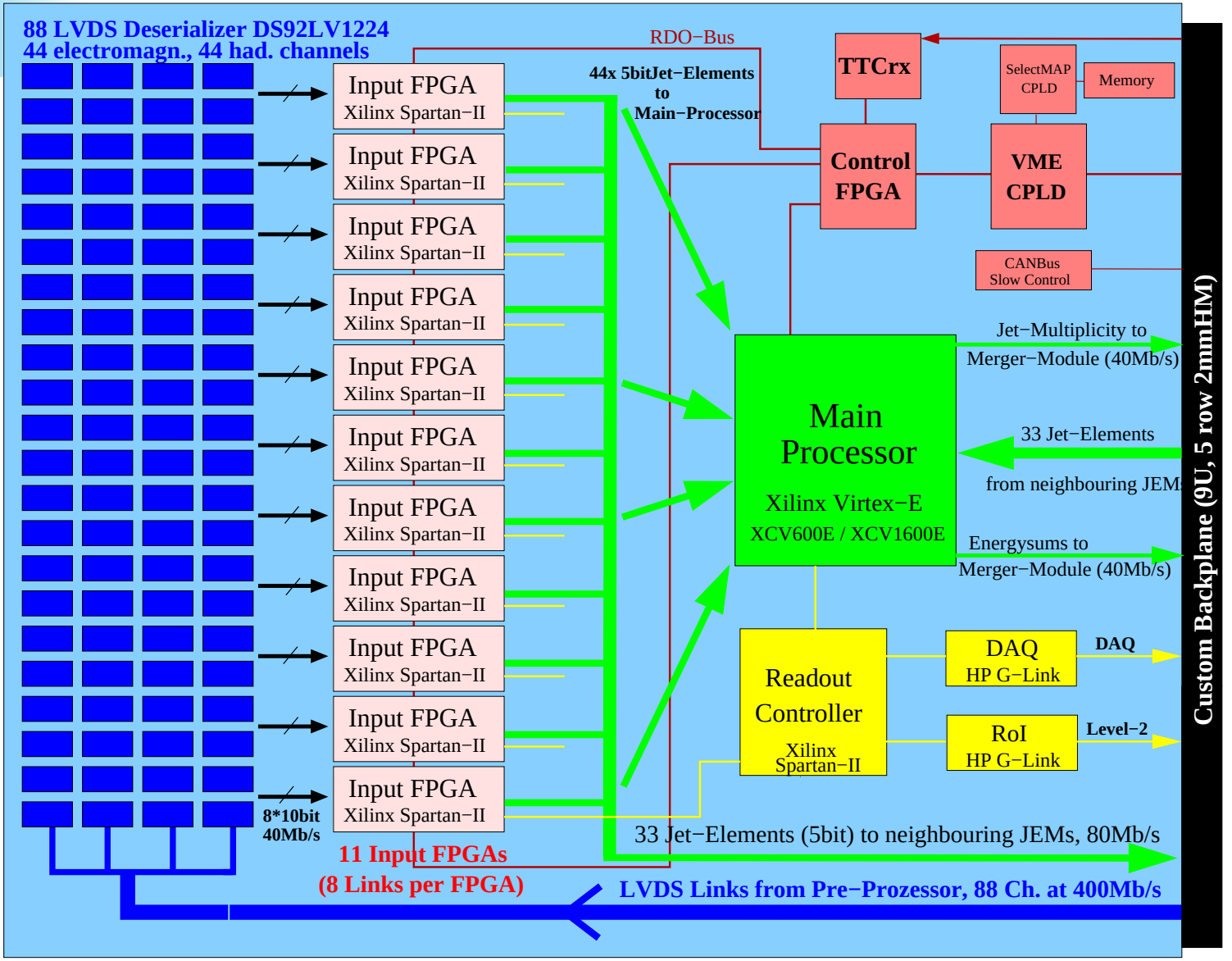
- Designed Mid-2000, Delivered Mid-2001, prototype version with 11 InputFPGAs and One-Channel LVDS deserialisers LV1224
- Version 0.1 has a XCV600E device as MainProcessor
- TTCrx on TileCal prototype daughtermodule, painfully debugged but now working reliably within TTC environment.

Testing status at QMUL meeting (report by Cano):

- Realtime Data Path for Energy Summation Algorithm successfully checked with test vectors (Random) fed from DSS (16 channels, two InputFPGAs), and also physics test vectors fed to on-board Playback Memories (64 channels of core region)
- Readout test not successful.

Jet/Energy Module prototypes:

JEM 0.1/0.2



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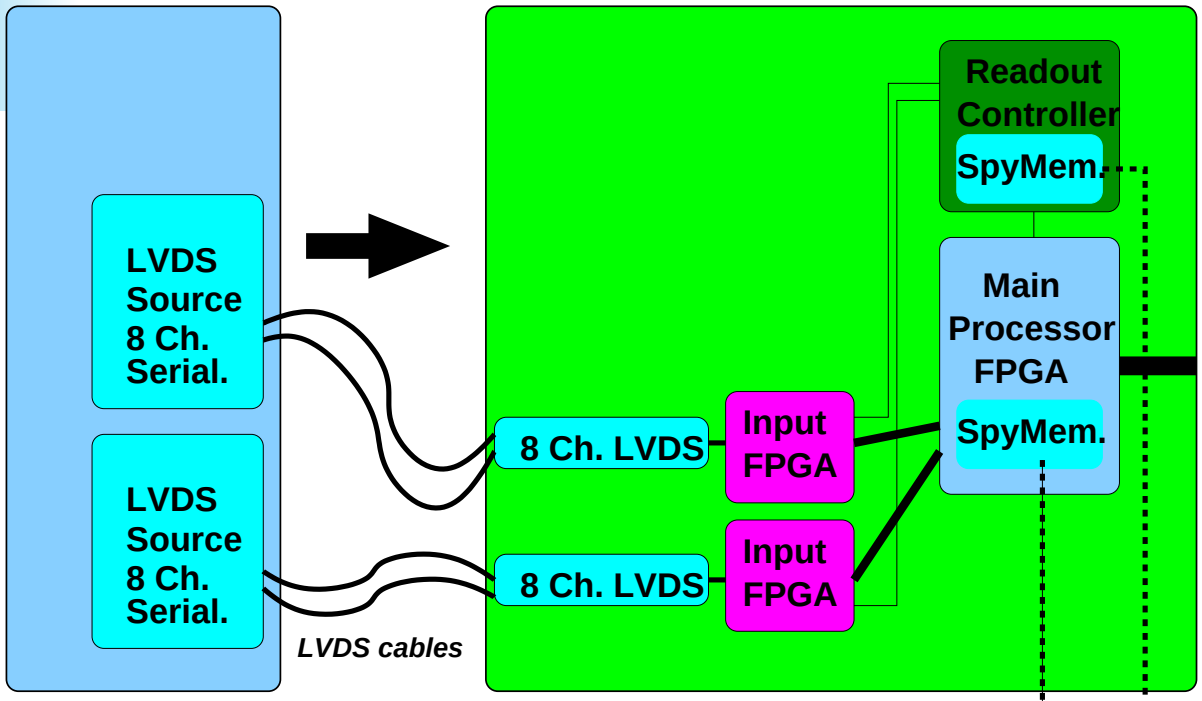
Since then...

- Hardware problems of one G-Link identified:
  only second one - labelled 'ROI G-Link' - works properly.
  Other one needs replacement.
- New set of firmware provided by Uli, most notably allows for readout of data coming from the Playback Memories. Allows for tests of all 88 channels in readout. Formerly only LVDS fed channels in readout.
- Simulation `jemSim` now includes Readout Stream for Slice Data
  Debugged within `dbSim`, connected to ROD within `cpRodSim`.
- Cano confirms correct readout functionality and stream format is provided by JEM, using Spy Memories within ReadoutControllerFPGA, comparing with `jemSim` dump.

Test of Jet/Energy Module with DSS LVDS data feed



DSS
Data Source/Sink Module
Modular test system

JEM
Jet/EnergySum Module
(only 2 of 11 InputFPGAs shown)

Random Data for 16 Ch. filled into DSS Data Buffers

Compare to Expected Results from Simulation

Results read from Spy−Memories

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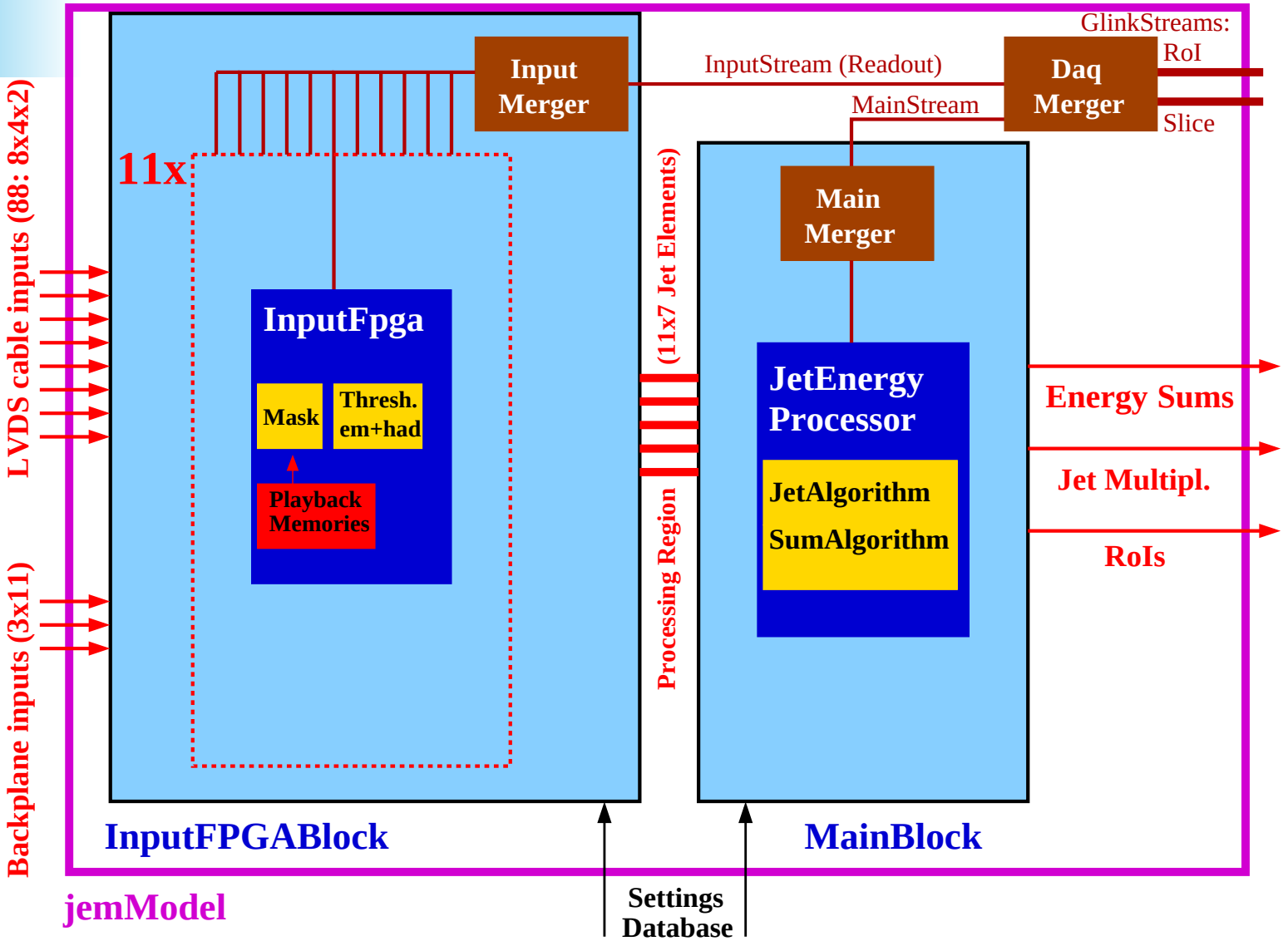
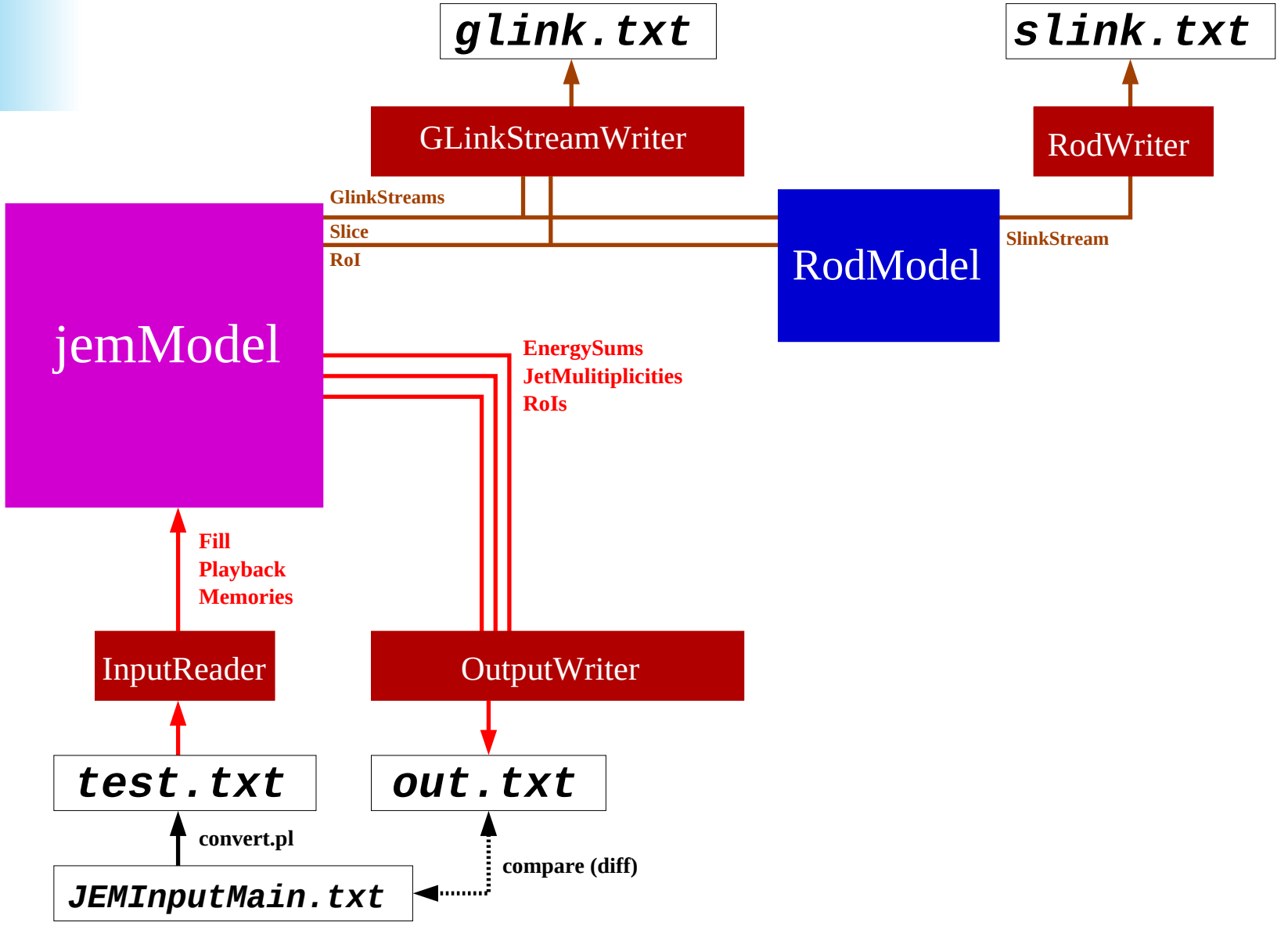
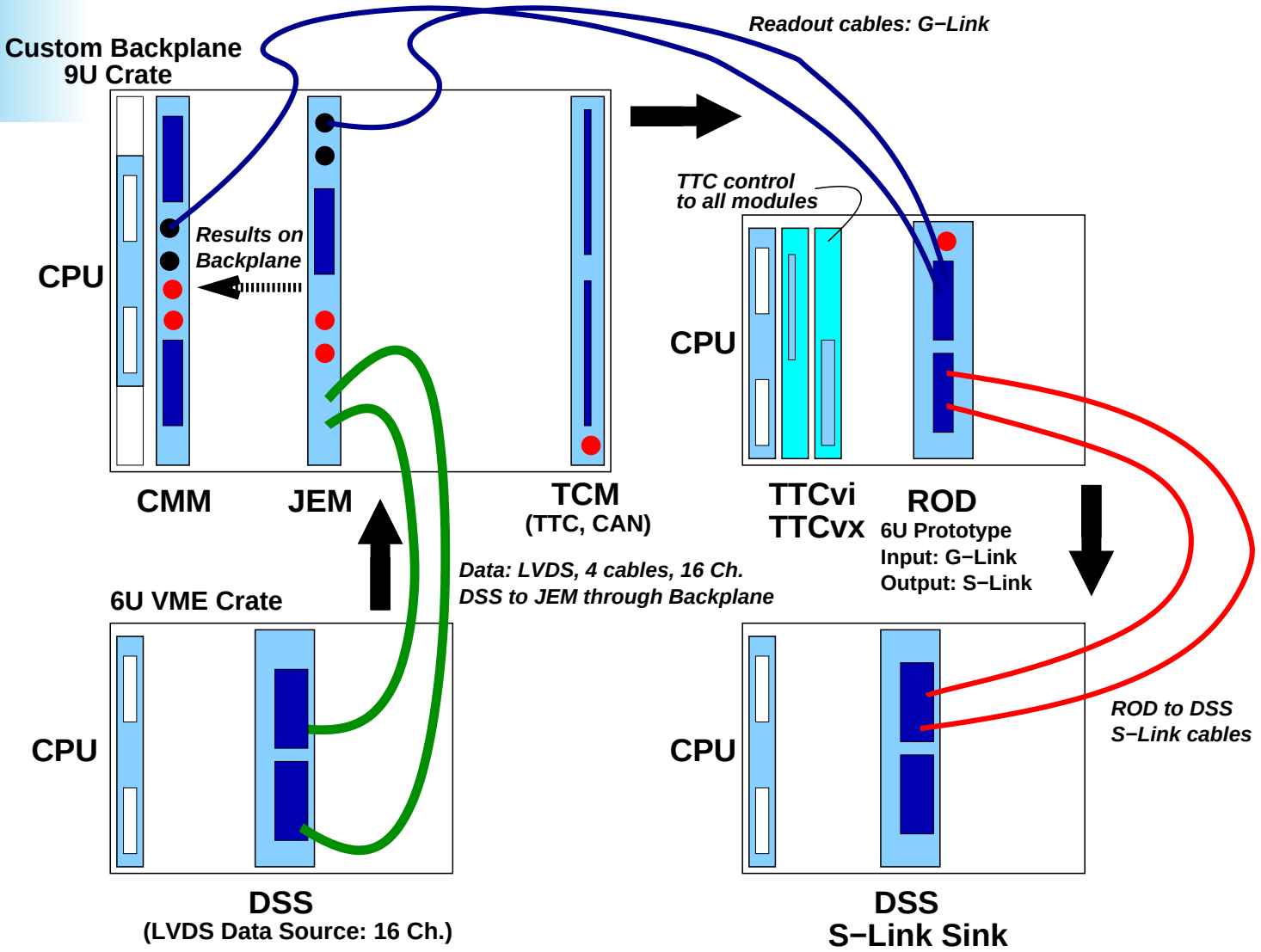
Architecture of jemModel *in* jemSim



Test setup for stand-alone simulation



Readout test at RAL (I): Test setup



run by Murrough, Bruce, Uli, Cano, Norman, Steve, Juergen

Readout test at RAL (II): Results

- Mapping issues understood, need to be sorted out in `jemSim`.
- Constant pattern for all 88 input ch. (Playback Memories) : Readout chain works correctly for several thousand events (hardware results equal simulation).
- Binary counting pattern on 16 LVDS input ch.: Readout of InputFPGA data as expected for 30000 events (constant offset).

Setup working properly in general.
No very long test performed yet .

Communication of JEM 0.1 to Merger Module

- Test vector used: 16 Ch. constant and counting pattern.
- Readout of CMM via ROD setup.
- Merger firmware: e/γ merging algorithm used.
- Current results: data patterns appear in CMM readout at correct place, but do not match expectation, seem somewhat arbitrary

Test ongoing, should continue after G-Link repair on JEM 0.1

What's next ?

I. Hardware Tests

- Discussion with Mainz/Stockholm on how to proceed with JEM prototype tests.
- Key issue: Availability of Jet-Algorithm for JEM prototype !
- Merger communication needs to be debugged properly, also with high statistics.
- Energy-sum Merger CMM: firmware is available. Simulation needs to be added to `cmmSim`. Perform hardware test using onboard memories (Esp. check funny LUT and saturation issues).

Thank you to all people involved in complex testing !!!

Test results on JEM prototype will be presented by Andrea at LECC 2003 in Amsterdam.

Please review proceedings.

What's next ?

II. Simulation

- Jet algorithm needs to be matched with Sam's code, already provided.
- Phi direction issue will be sorted soon (sorry for delay).
- RoI readout stream will be added.
- Data Generator to replace scripts needs to be added.
- Synchonise counting patterns (bunch counting ?), hardware to `jemSim`
- Physics test vectors: Replacement for old Atlfast-Fortran runs: Dump Jet Elements and Trigger Towers from `TrigT1Calo` interfacing `Atlfast-Athena`. Initial work started with Ed at CERN, interest by Stockholm group.