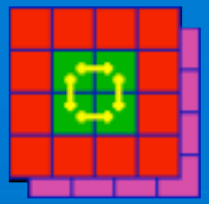
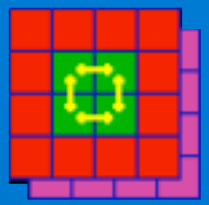


Readout Drivers

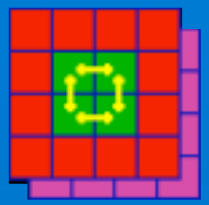
(L1Calo 6U Prototypes)

Current Status



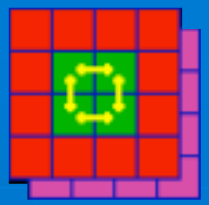
Overview

- Firmware Status
- Firmware Issues
- Hardware Status
- CPM, JEM and CMM Integration
- ROD Readout
- ROS Hardware



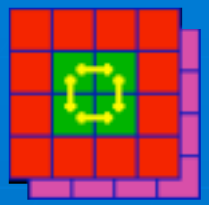
Firmware Status

- CP Data : Stable
  - **CP-Slice-16**: Bit 23 set in hit data words. — done
  - **CP-Slice-17**: Treatment of PP->CPM statusBits (S-ink trailer and hit words) — f/w specification and implementation
- JEM Data: Stable
  - Assembly ok. Multi-slice operation ok. — done
  - Formatting Mods (Crate ID) required — f/w specification and implementation
- CP RoI : Stable — done
  - Flow control needs to be confirmed — testing
- Cmm Cp Data: Stable
  - **CpCmm-Slice-1**: Various Bit field errors — robust?
- JEM RoI: in Progress — testing
  - **Jem-RoI-1**: Zero suppression behavior understood
  - James awaiting feedback
  - Other tests and extensive lake studies have delayed.



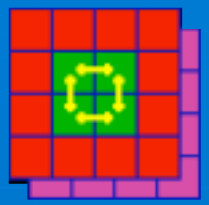
Firmware Issues

- New Designs:
  - James awaits specification for 4/5 CMM variants:
    - CMM JEM Slice Data
    - CMM JEM RoI
    - CMM Energy Slice Data
    - CMM Energy RoI
- Existing Designs:
  - Specification Errors
  - Formats require rationalisation
    - Started but stalled



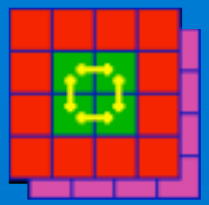
Hardware Status

- Tested and needing refurbishment:
  - S/N 1,2,4,7:
    - 1&2: Tested extensively (CP Slice and RoI)
    - 4&7: Tested except for flow control/ Dual S-Link operation.
  - Refurbishment means:
    - New G-Links Daughters
    - TTCDec replacement (when TTC fanout available.)
- In-System:
  - S/N 3,5,6,8
    - Modules have
      - New Generation G-Link Cards
      - Redesigned TTCDecs (2-pin lemo inputs, no longer require special interposer daughter card for assembly)
    - Equipped with JEM-Data, CPM-Data, CPM-RoI and CP-CMM firmware
- G-Link Problems:
  - Better understood and more stable links.
  - Long term optical solution.



CPM, JEM and CMM Integrations

- Readout:
  - One channel of one ROD.
  - L1A and orbits generated by DSS/GIO (controlled by simulation.)
  - Kicker acquires and compares events.
- CPM:
  - Data: Simulation and Hardware consistent. Aligned.
  - RoI: Simulation and Hardware consistent. Alignment understood.
- JEM:
  - Data: Simulation and Hardware aligned,
    - but channel mapping to be understood.
  - RoI: H/W output not available.
- CMM:
  - Initial tests:
    - With JEM: Work on understanding simulation and hardware underway
    - With CPM: CPM available … initial tests at RAL and Birmingham (?). To continue
- Future:
  - Multiple module:
    - Operation and consistency checks.



Rod Readout

- Issues in Triggering:
  - Busy Handling
    - Either
      - Wrap playback memories around each orbit, in which case current DSS/GIO BUSY strategy of delaying start of new trigger-orbit sequence until BUSY deasserted is ok.
      - Wrap-64. Re-implement DSS BUSY strategy so that empty orbits follow trigger-orbit sequence and BUSY results in an increment by 64 of the emtpy orbit count.
    - Testing
    - Interaction with CTPD.
    - Single BUSY module prototype could be available in October.
      - To be negociated with Per Gallno
- ROS:
  - Currently, readout proceeds via the DSS.
  - Need to be able to readout with ROS:
    - 8+1 links in one PCI machine
      - Issue: CTPD, as is, can't use FILAR.
    - New H/W available Mid October. Need to commission ROS with ODIN hardware by then:
      - ROS exercise.
      - Intermediate solution.

ROS Hardware

- HOLA Source S-Link Source
  - Single fibre-pair version of ODINS.
    - Require 3.3V signalling and 3.3V power:
    - Birmingham designing adapter board.
- FILAR quad S-Link Sink
  - Accommodate 4 HOLAs (3.3V PCI)
  - 66 MHz / 64 bit, so 4 times bandwidth of old PCI interfaces.
- ROS:
  - New fast box with
    - 4 independent PCI-X busses (6 slots)
    - Dual Processor: 3 GHz
    - GC-LE chipset