Step	Test	Items required	Provided by
0	Infrastructure	9U powered Processor crate with backplane	RAL
		Fan Tray	RAL
		VMM (for 9U crate)	RAL
		TCM (for 9U crate)	RAL
		Concurrent CPU	RAL
		6U powered VME crate	RAL
		Fan Tray	RAL
		Concurrent CPU	Stockholm
		VME Display	RAL
		TTCvi	Mainz
		TTCvx	Mainz
		Pulse Generator	RAL
		CBD (triggers pulse generator)	RAL
		Optical Fibres (how many)	
		Electrical Fanout??	
		Computer Monitor & Keyboard	RAL
1	Set up TTC system (TTCvi, TTCvx) for clock distribution only		
2	Repeat standalone tests JEM0.1 / energy paths only (within crate environment, if possible)	Jem 0.1	Mainz
		TTCrx daughters (2)	Mainz
		Bench Power Supply	RAL
3	Repeat standalone tests JEM0.2	Jem 0.2	Mainz
4	Test the jet code (playback,spy) in core region		
5	Fully integrate DSS and JEMs in the TTC environment	DSS	Mainz
		LVDS Serial Daughterboards (2)	Mainz
		TTCrx Test Card	Mainz
		LVDS Cables	Mainz
6	Run the input synchronisation software and adjust the input signal latency (full JEP = 2 JEMs)		
7	Run a delay scan to determine the optimum sampling phase of the FIO inputs		
8	Test FIO data transfer and determine low level errors for the full JEP		
9	Connect JEM G-links to either a DSS or a ROD to test the slice / ROI data paths		
		DSS G-link Rx daughterboard	RAL (MfG)
		ROD	RAL (MfG)
		JEM DAQ firmware	Mainz
		JEM RoI Firmware	Mainz
10	Test JEM-merger data transfer	CMM emulator	Birmingham
		DSS GIO parallel LVDS input daughtercard	RAL (Mfg)
		CMM (e/gamma firmware sufficient)	RAL (Mfg)
11	Test energy merger	CMM Energy firmware	Mainz
		ROD, CMM Energy readout/RoI firmware	RAL
12	Test jet merger	CMM Jet firmware	Stockholm
		ROD, CMM Jet readout/RoI firmware	RAL