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Testing – Discussion Initiator

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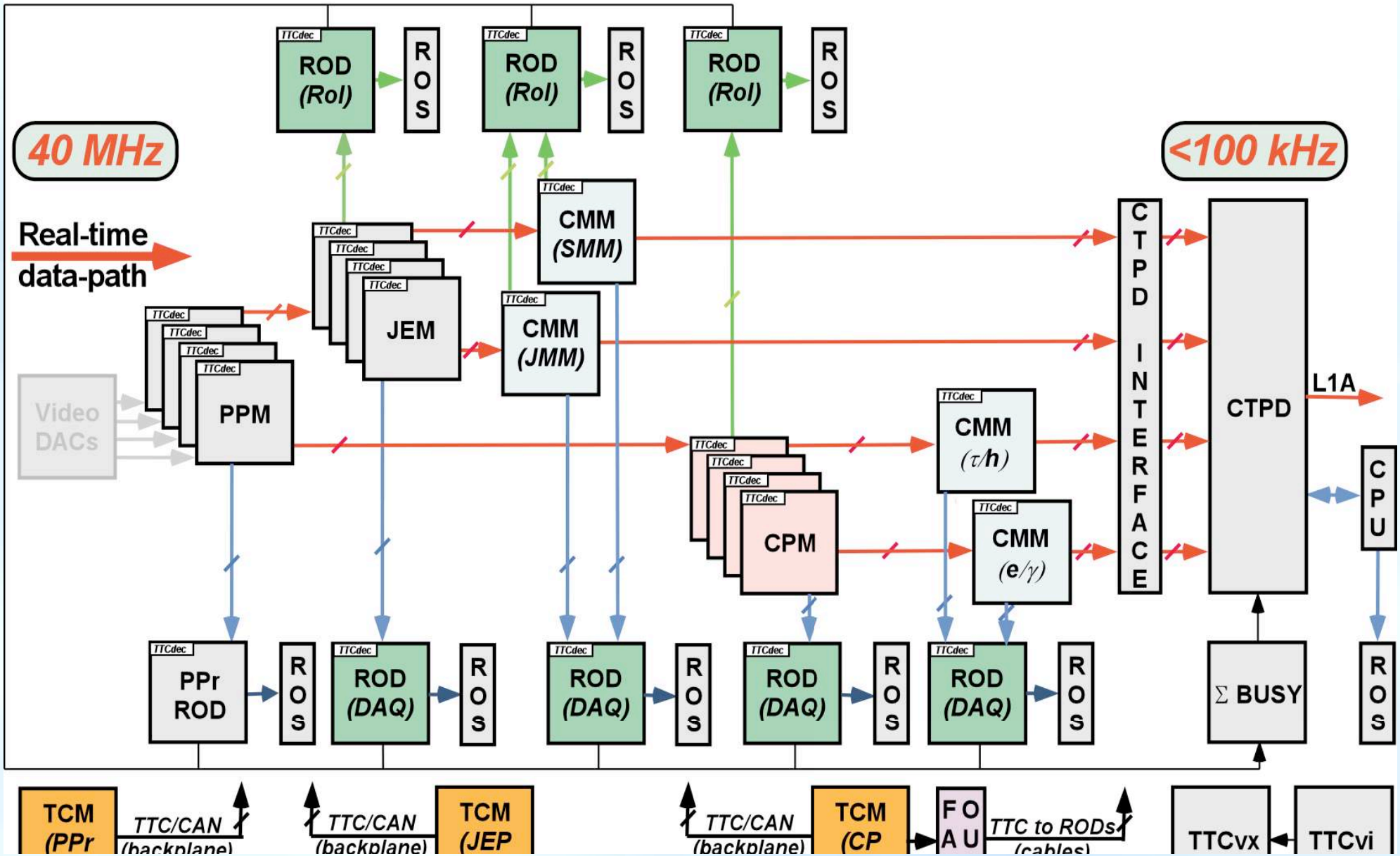
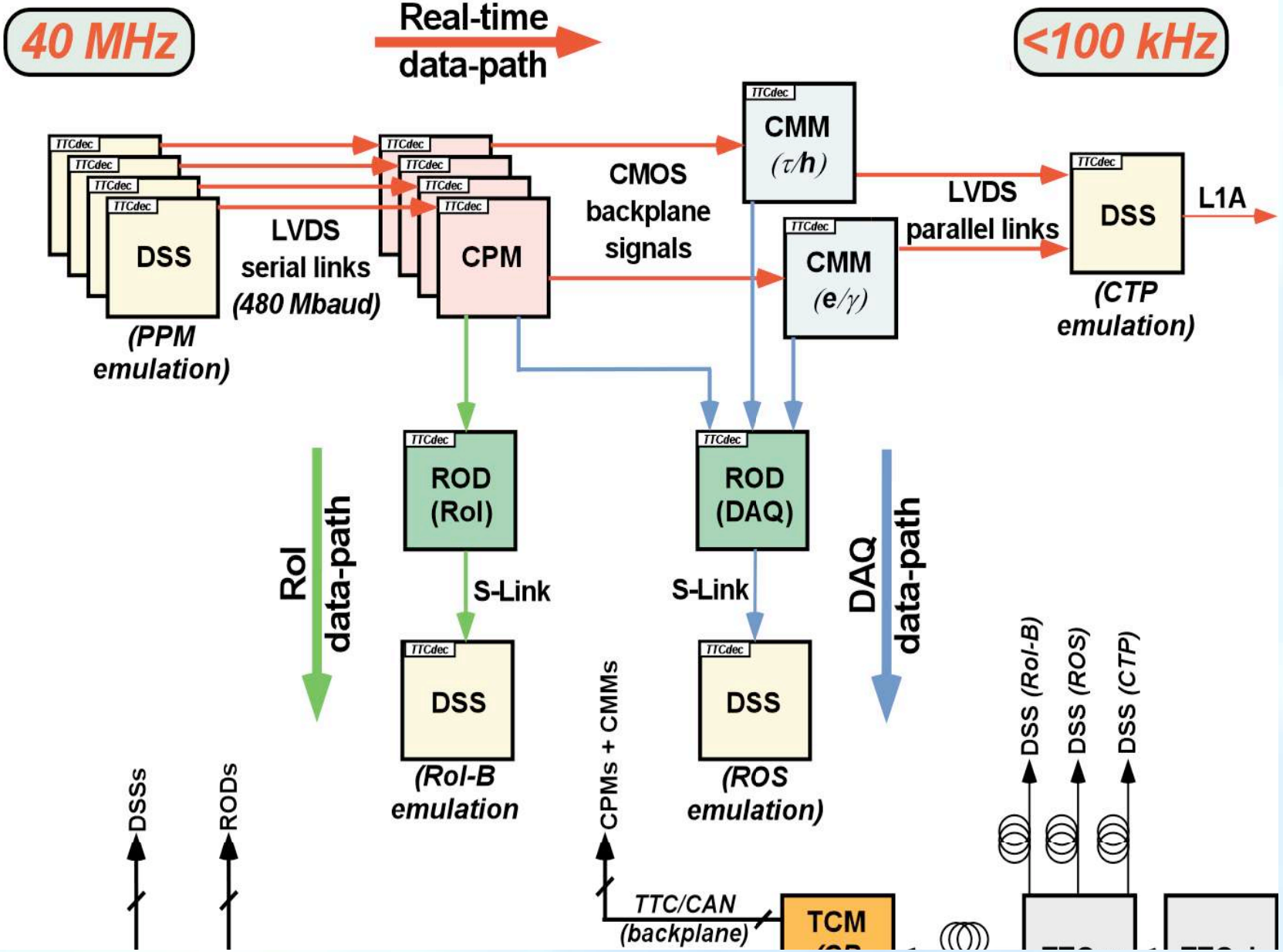
ATLAS Level-1 Calorimeter Trigger
Full System "Slice" Tests (Heidelberg: Q1-Q2 2003)



ATLAS Level-1 Calorimeter Trigger
Sub-System "Slice" Tests (UK: Q3-Q4 2002)



JEP Tests (1)

Step	Test	Items required	Provided by
0	Infrastructure	9U powered Processor crate with backplane	RAL
		Fan Tray	RAL
		VMM (for 9U crate)	RAL
		TCM (for 9U crate)	RAL
		Concurrent CPU	RAL
		6U powered VME crate	RAL
		Fan Tray	RAL
		Concurrent CPU	Stockholm
		VME Display	RAL
		TTCvi	Mainz
		TTCvx	Mainz
		Pulse Generator	RAL
		CBD (triggers pulse generator)	RAL
		Optical Fibres (how many)	
		Electrical Fanout??	
		Computer Monitor & Keyboard	RAL
1	Set up TTC system (TTCvi, TTCvx) for clock distribution only		
2	Repeat standalone tests JEM0.1 / energy paths only (within crate environment, if possible)	Jem 0.1	Mainz
		TTCrx daughters (2)	Mainz
		Bench Power Supply	RAL
3	Repeat standalone tests JEM0.2	Jem 0.2	Mainz

JEP Tests (2)

5	Fully integrate DSS and JEMs in the TTC environment	DSS	Mainz
		LVDS Serial Daughterboards (2)	Mainz
		TTCrx Test Card	Mainz
		LVDS Cables	Mainz
6	Run the input synchronisation software and adjust the input signal latency (full JEP = 2 JEMs)		
7	Run a delay scan to determine the optimum sampling phase of the FIO inputs		
8	Test FIO data transfer and determine low level errors for the full JEP		
9	Connect JEM G-links to either a DSS or a ROD to test the slice / ROI data paths		
		DSS G-link Rx daughterboard	RAL (MfG)
		ROD	RAL (MfG)
		JEM DAQ firmware	Mainz
		JEM RoI Firmware	Mainz
10	Test JEM-merger data transfer	CMM emulator	Birmingham
		DSS GIO parallel LVDS input daughtercard	RAL (Mfg)
		CMM (e/gamma firmware sufficient)	RAL (Mfg)
11	Test energy merger	CMM Energy firmware	Mainz
		ROD, CMM Energy readout/RoI firmware	RAL

CP pre-subslice-assembly tests (1)

- **"Stand-alone" (to make sure individual modules work)**
  - CPM
    - ***Individual module internals;***
    - ***LVDS input from DSS, including all channels together;***
    - ***160 Mbit backplane (3 CPMs) – timing, signal quality;***
    - ***TTC Interface***
    - ***G-Link output to DSS (slice, RoI) in response to L1A***
    - ***Realtime Hits via CMM emulator to DSS/GIO – timing, signal quality***
    - ***Software – module service, simulation, test vectors,…***
  - ROD (for each data variant)
    - ***TTC interface***
    - ***G-Link input from DSS, S-Link sink to DSS***
    - ***Reformatting details, Zero Suppression, Busy***
    - ***S-Link to ROS***
    - ***Software – module service, simulation, test vectors,…***

CP pre-subslice-assembly tests (2)

- **"Stand-alone" (continued)**
  - CMM (which also has other variants)
    - ***Module internals***
    - ***Realtime Hits from DSS/GIO via CPM emulator – tming, signal quality***
    - ***Sums to DSS/GIO***
    - ***Crate/System link***
    - ***TTC Interface***
    - ***G-Link output to DSS (Slice, RoI in other variants)***
    - ***Software – module service, simulation, test vectors,…***
  - DSS
    - ***L1A generator firmware***

Pairs of modules

- **Intermodule timing and Integration**
  - CPM – CMM via backplane: timing, signal quality
  - CPM – ROD (slice, RoI) - ROS
  - CMM – ROD (slice) - ROS
  - Custom Backplane systematic check
    - ***VME--, 160 MHz, hits, TTC, CAN - all at every slot, and crosstalk.***
  - Check of TTC synchronisation commands if not done already
  - Multimodule software, including run control, databases, event processing

Channels and Modules

- **Individual module tests need every input & output link to be concurrently active and searched for strange effects, and with all firmware variants**
- **Sub-slice and Full slice tests need at least enough data to fully populate 1 cluster window + 1 Jet window**
  - but with at least one copy of all firmware variants of all modules working concurrently.

To complete prior to Full Slice

- 6U ROD firmware variants
- Event building (ROS …)

- Tests of a CPU or DSS daughter on a ROD (?)
- CanBus system (to be fully defined)
- 9U ROD
- Timing Calibration software (analogue/digital)

ROS and RoIB and CTPD

- **ROS is essential for tests and in constant use for event building for all subslice and slice testing involving RODs.**
- **RoIB can be tested when convenient:**
  - need RoIB, + all modules providing RoIs, + agreed strategy for them to interface to our testing environment & run control.
  - Can be removed once test is complete.
- **CTPD can be integrated once at least 1 CMM works**
  - But will then provide L1A and should stay till slice is complete.
  - Timing will change as other modules are added

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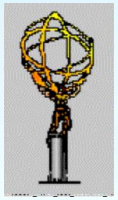

Over To You