CPM Testing

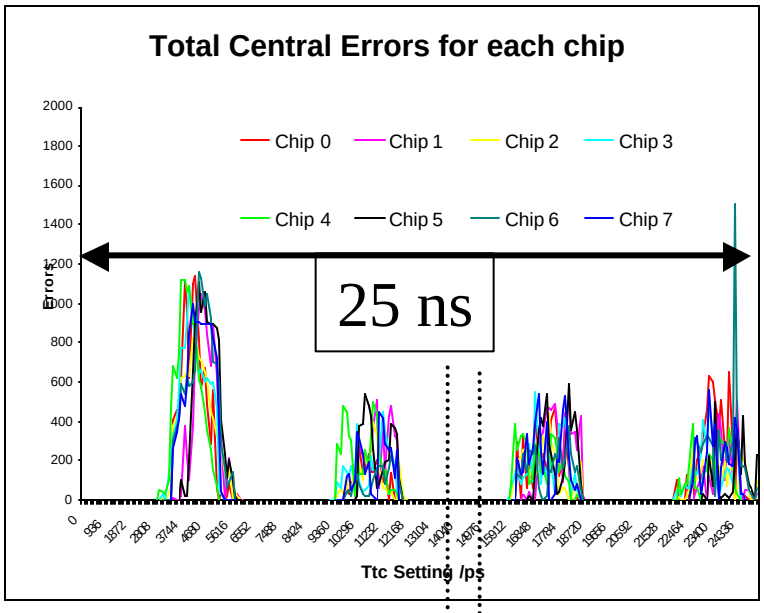
UK Meeting, Thursday the 27th of February 2003

Real Time Data Path Test: SRL chip to CP chip

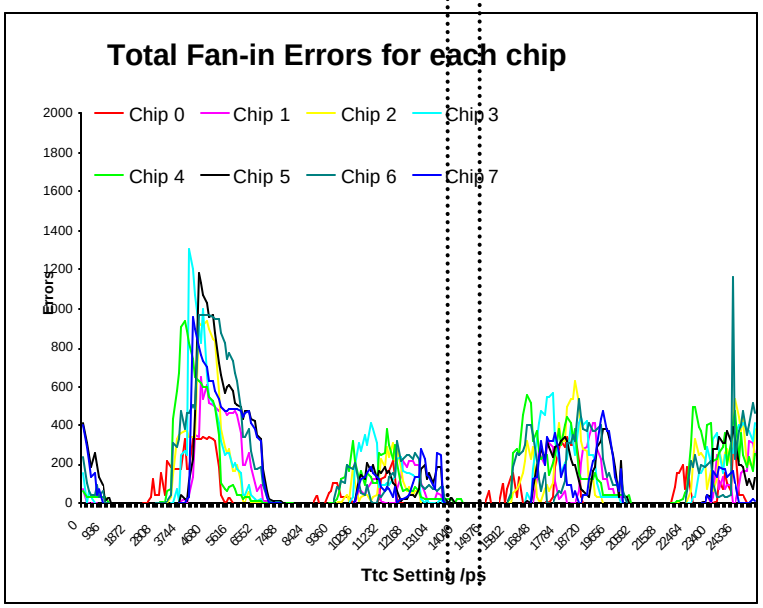
- CP Chip loaded with 2 one phase:
  - One phase for on board signal
  - One phase for backplane signal
- Srl Chip loaded with new F/W, isolating access to VME when reading memory
  - Cure data corrupted seen in RAM (thanks Ian)
- Perform time scanning by changing phase between CP and SRL

SRL chip to CP chip: Result

- Recovered the 4 periods of the 160 MHz data stream
- Onboard clock rerouted for CP chip to match BP error free period
- BP signals are spreading more due to integrity of signals



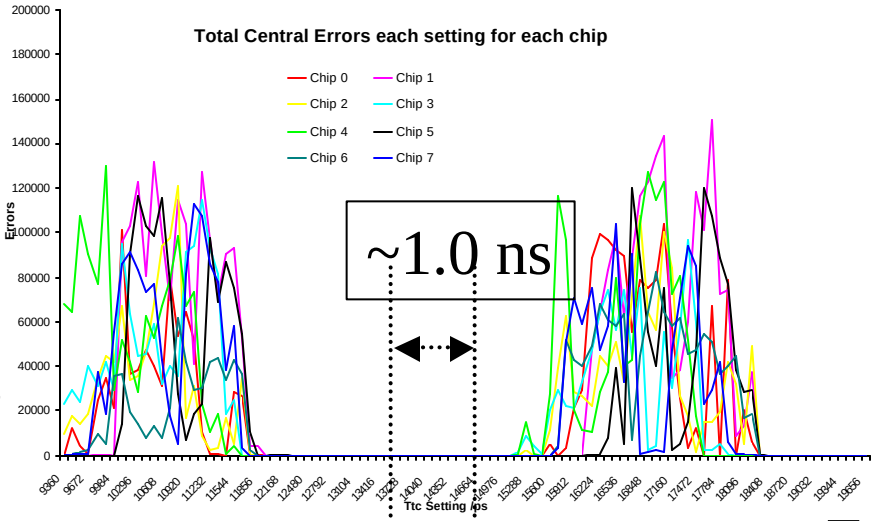
OnBoard Data



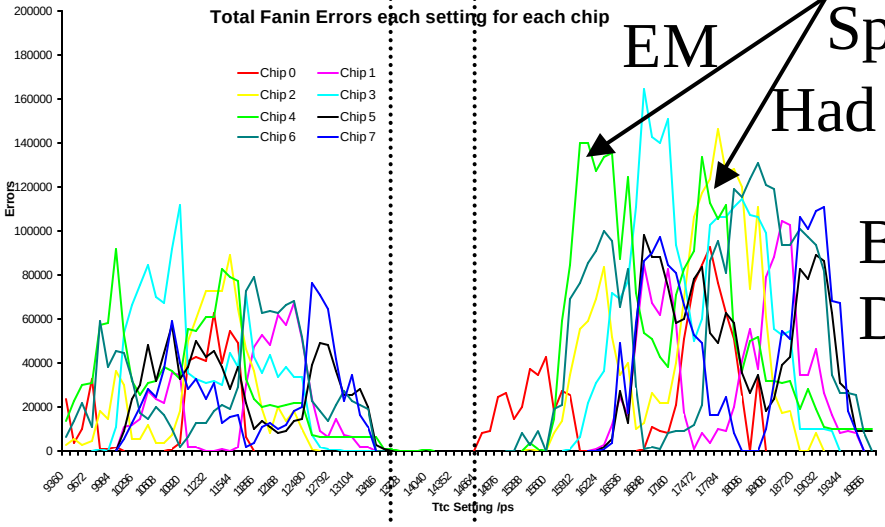
Backplane Data

SRL chip to CP chip: zoom on result

- Time window where CP and SRL work is as wide as 1 ns
- Overnight run shows no errors
- Only 90% of data are looped back
- Extra CPM will enable to test all backplane link



OnBoard Data



Example of Spread EM Had

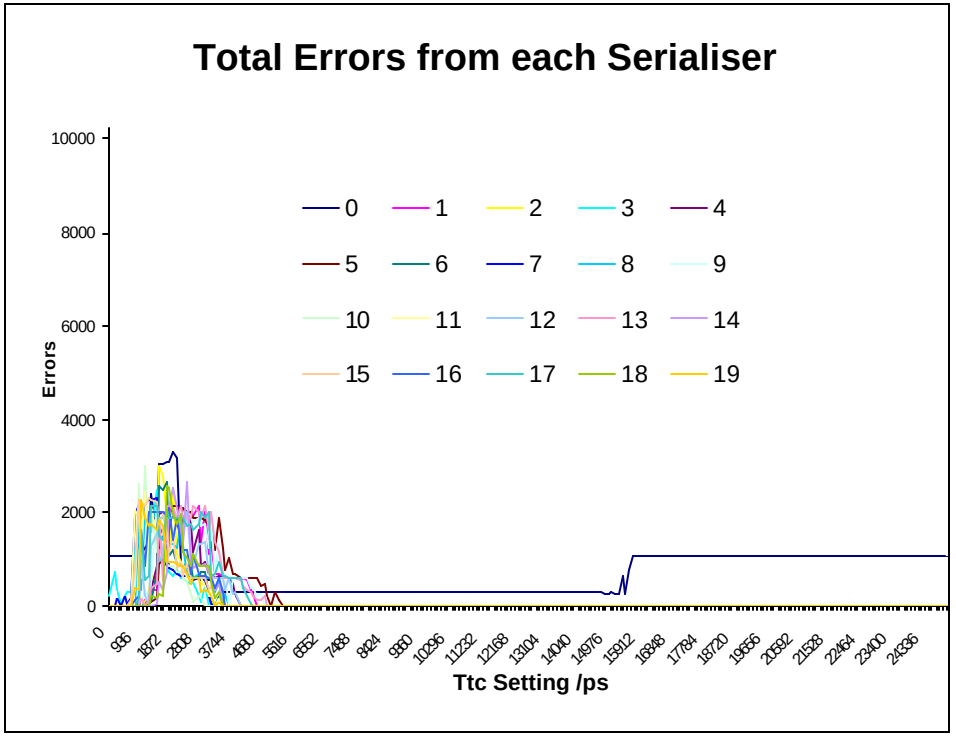
Backplane Data

CP F/W choice

- Two “one phase” method is working, testing with algorithm also show no problem
- One F/W designed for an upgrade 7 of the same device has been on trial on present chip
  - First results by eyes looks encouraging but…
  - …we don’t know if we can fit the algorithm inside
- CPM#1 board is working for the slice test, a CPM#2 with exactly the same component (ie same CP chips devices) is strongly flavored for a second working board.

Real Time Data Path:LVDS data to Serialiser

- 80 serialisers locked
- Perform timing scan by changing clock on Serialiser
- Stable over ~20 ns
- Only one serialiser shows some problems:
  - One pin of one Lvds Rx not soldered: strobe on opposite edge of other receivers
- Overnight Run?



DSS problems seen

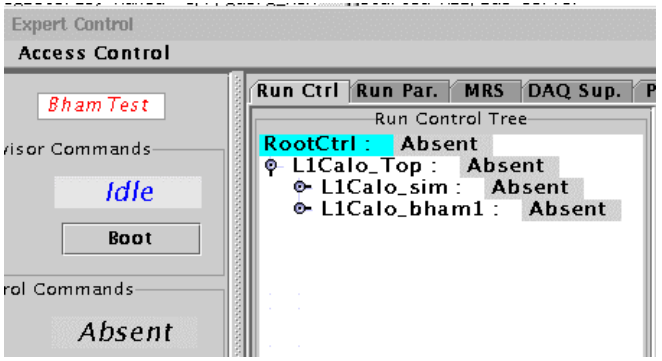
- We were using the TTC Broadcast command to start the output of data from the DSS
- Bit read need to be kept high (bcrst[6] and bcrst[7]) in order to keep data generated
- But it’s a broadcast command, previous bit are gated with a strobe , which goes down after a while, leaving bcrs[] floating, and going low eventually
- Output data stopped to be generated: Dss need to handle the strobe to avoid it

Access to F/W sources

- Access to part of the serialiser source was very helpful to generate a source for ChipScope and a BitErrorRater Tester for LVDS Rx
- Access to Cp F/W in similar way, we might also think of a BER for the CP Chip.
- Useful when designer on vacation and quick fix needed (bit wrongly expected high)

CPM Tests Integrated with Run Controller

- RC can deal with previous test modes
- Still a lot of work to be done :
  - Loading of F/W from database to be done
  - Setting thresholds, mask
  - …(discover everyday)



Next step: testing ROC – HIT output – CP algorithm

- Roc and Hit test could be done by using RAM available in ROC
- More test will need at least an extra DSS for reading Glink output, GIO card and new TTCdec card
- 2 more CPMs will enable fully testing of the algorithm
- Measure of latency

Discussion Items

- CPM assembled with same CP chip as the first one
- Total of 6 DSSs for B’ham for early tests, and GIO, and TTCdec
- Access to F/W source code
- New PCBs to be build, instead of cleaning old ones