CPM Prototype Hardware

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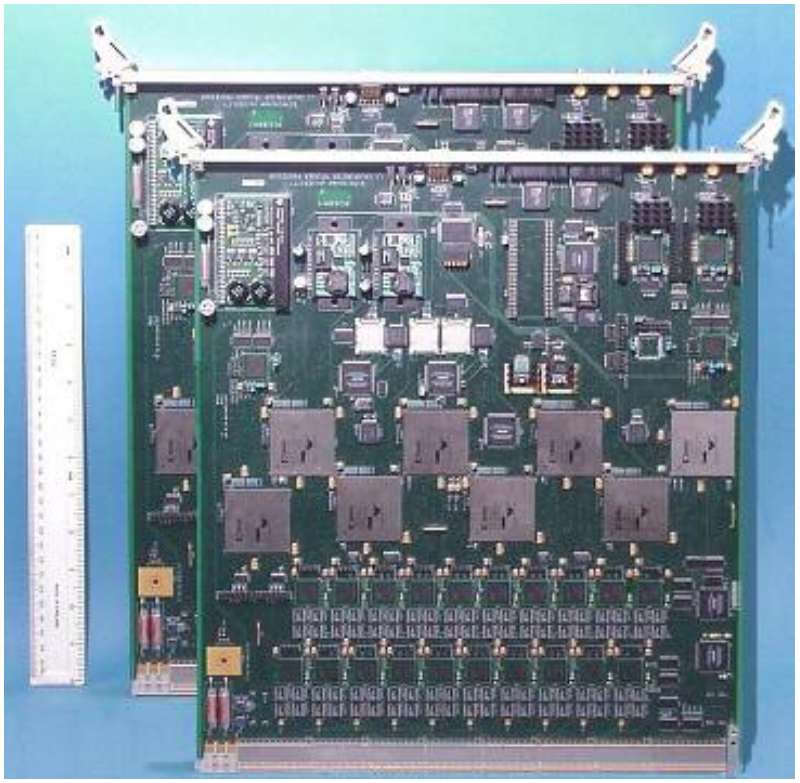
- Summary



R. Staley

Hardware Status

CPM#1 - Assembled , working and in use at Birmingham for evaluation tests.

CPM#2 - Assembled. JTAG testing showed problems with assembly. Poor soldering of some of the large FPGAs. PCBs are 1 year old.

Possible surface contamination of PCB and/or leaching of the protective nickel plating.

CPM#3 & CPM#4. - PCBs have been cleaned. Can these be used?

CPM#3 to be fully assembled = CPM#1.

160 Mb/s Links (1)

FPGA issues.

The 4-phase calibration scheme doesn't work with the -6 speed grade of Virtex-E used on CPM#1. DLLs are not fast enough to generate 4 phase clocks + …

Currently using a dual 1-phase calibration scheme which seems to be working. (Results from Gilles, Steve and Christian).

Revised 4-phase design may also need larger size Virtex-E.

...but remember next CPM design will use Virtex-2 .

160 Mb/s Links (2)

PCB issues.

Signal integrity not ideal, due to PCB layout 'mistakes'.
Auto-router was used.

Reduced Timing margins seen on some inputs to CPM#1 will affect both 1-phase and 4-phase schemes.

LVDS source module (1)

A 44 or 88 link LVDS source for testing CPM and JPM.

80 links would replace 5 DSSs and completely drive 1 CPM.

- Standard 6U VME module.
- Driven by Onboard Oscillator , external clock or TTCdec.
- TTCdec input optical or electrical.
- 1K x 10bit memory driving each link.

LVDS source module (2)

Choices:

1. Standard LVDS - 44 links (easy)
2. Octal LVDS in BGA - 88 links
3. Virtex2 FPGAs - 88 links

Estimated Component Cost (excludes PCB and connectors):

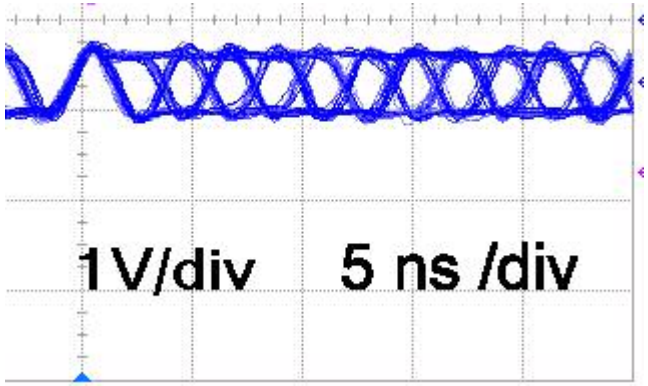
Choice 2 = $1200
Choice 3 = $ 500

LVDS source module (3)

Virtex2 as 480Mb/s LVDS source.

DLLs clocking data at 240MHz, then combined using DDR I/O.

Quick test using V2 demo board:



480Mb/s data.

Power Supplies

- Birmingham PSU fitted with delay circuit - 3.3V supply turns-on long after 5.0V supply has powered-up.

- Mains filter added.

9U crate powered-up 20+ times without affecting neighbours.

All power supplies to be modified.

Summary

Still testing CPM#1.

- Capturing 160Mb/s data using single-phase calibration.
- Poor quality of some backplane links.
- CPM #2. Assembly issues. Some BGAs not soldered correctly
- CPM #3 to be fully assembled with -6 grade FPGAs as #1

Still no show-stoppers.