Conclusions:

1. There is a modest overshoot for the LAr Calorimeter latency (10%), but this figure needs confirmation. Estimates will be obtained for the equivalent TileCal figures, and some measurements may be possible w/b 16th June at CERN.

The Patch-Panels for the TileCal appear to be a cabling nightmare - unintended increases in latency must be avoided.

2. The PPr is comfortably within its envelope (partly because of the chosen FADC chips), and these are measured figures.

3. The CP exceeds its latency envelope by nearly 60% (8.3), and most of that excess appears to be within the CP FPGA, with 8.4 BC. The firmware must be looked at very carefully to understand how this figure is constructed and to see if it can be significantly reduced.

The latency figures for the new CPM1.5 design will be relatively unchanged.

The CMM figures should be confirmed by actual measurements if possible.

4. The JEP (Energy) is currently comfortably inside its envelope (by 15%). The corresponding Jet figures should be obtained as soon as possible.

In the new JEM1 design there are possible reductions of 0.5 in the Input FPGAs. However, there are potential increases due to the automatic phase adjustment circuitry for data synchronisation.

5. The CTP figures require updating - e.g. the board architecture has changed since the May 2000 estimates.

6. Tony will prepare and update a working spreadsheet to keep monitor these figures.

7. A single definition of latency estimates/measurements must be made, and used by each sub-system to avoid zero/double counting in the interface regions.