Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 8th April 2004

Birmingham: **John Garvey*, Steve Hillier, Richard Staley, Pete Watkins**

Heidelberg: **Ralf Achenbach, Florian Föhlisch, Paul Hanke, Eike-Erik Kluge, Karlheinz Meier, Pavel Meshkov, Frederik Rühr, Klaus Schmitt, Hans-Christian Schultz-Coulon**

Mainz: **Stefan Rieke**

RAL: **Bruce Barnett, Norman Gee, Tony Gillman, Weiming Qian**

Stockholm: **Attila Hidvégi, Sam Silverstein**

******at RAL*

1. Birmingham

- Successful commissioning of the two CPM1.5 modules has progressed extremely rapidly. The clocks from the TTCdec exhibit no deterministic jitter, and the quality of the 160 Mbit/sec backplane signals is much better than on the CPM1.0 modules.
- However, the backplane data timing margins are tighter than expected, because the complex routing demanded by the extremely high track density has produced large variations in propagation delays, although only a small number of traces have excessive lengths. The possible need for one extra backplane timing clock was fortunately foreseen and therefore provided on the PCB, but the CP FPGA firmware will need some modifications to use it for selected input channels. Gilles has started to look at the necessary changes, which will hopefully be ready for testing by the end of April.
- The optical links fed from the CPM1.5 G-link outputs work correctly.
- The data format from the PPM into the CPM differ from that expected by the Serialiser FPGA firmware, with the Parity and BCMux bits shifted and with the data bits in reverse order in the serial LVDS bitstream. In principle, this can be corrected by redefining the Serialiser input pins, hopefully without introducing timing delays. Ian will look at what changes are needed in the firmware.
- Tamsin will soon be ready to test the firmware patch for the CPM Serialiser and CP FPGAs, which will correct the "odd-parity/zero-data" error present in the PPr ASIC1.0.

2. Heidelberg

- The new PPr ASIC1.1 has successfully passed all its tests, and five MCM substrates which have been loaded with the new dies are now working.
- Wurth is expected to deliver 55 new MCM substrates, using FR4 material, at the beginning of May.
- In order to minimize delays, a provisional order for the full production quantity of the new PPr ASIC1.1 wafers has already been placed, but there is a cancellation period allowed if problems were to arise during the next eight weeks. As previously proposed, the PRR for the MCM will treat it as a single testable "component", so there should be no need for a separate PRR for the ASIC. Paul will discuss this further with Philippe Farthouat, with a view to holding the MCM PRR some time in May, after a sample of the new FR4 substrates have been loaded with PPr ASIC1.1 dies and successfully tested.
- It is proposed to test the "upstream" analogue data path in the PPM in the ATLAS Combined Test-Beam run in June this year, in order to prove this part of the architecture before the

intensive Test-Beam run in September. This will involve a relatively simple set-up of PPM, "home-brew" processor and LAr/TileCal receiver, all housed in a VME64x crate, with which particle- and calibration-generated calorimeter signals can be written to the 3μsec PPr ASIC pipeline memories on receipt of a beam trigger (equivalent to a Level-1 Accept), and then read back to a file. Most of this system is what was used in the recent LAr receiver tests in Heidelberg, and the only piece still incomplete is the firmware for accessing the PPr ASIC on the MCM., which Kambiz has almost ported to the ReM FPGA. Further discussions will be held with Bill Cleland et al to establish a working plan. As the Test-Beam co-ordinator, Norman will negotiate our participation.

- There are another three PPM PCBs available at KIP, which will be supplied to two different companies for assembly this month, making a total of four modules available in May.

3. Mainz

- Bruno has started to test three more Input daughter-cards for the first JEM1, which have been assembled and delivered.
- The first G-link daughter-card will be assembled by Bruno.
- VME access to the JEM1 CPLD and Sum/Control FPGA is working, but the Input and Jet processors have not yet been configured.
- The new TTCdec produces the appropriate clocks, but TTC control from the FPGA is not yet implemented.
- Stefan and Andrey are currently trying to get the CAN processor working.

4. RAL

- The 9U ROD module layout is progressing well, and the board is already looking very "busy".
- We send James our best wishes for recovery from his recent accident. It is possible that he will be back at RAL quite soon. He had almost completed partitioning the 9U ROD design, and there will be a planning meeting next week to allocate people to firmware tasks.
- The KVASER PCI CANbus card has now been ordered from the UK distributor to provide Adam with a similar set-up to that of Andrey in Mainz.
- There has been a rationalisation of the general TTC command structure.

5. Stockholm

- Attila has almost completed the Jet FPGA firmware. All functionality is complete, but he still has to define the mapping of the inputs, which he needs to discuss with Uli.
- Sam proposes to use two different cables for linking the Crate and System Jet CMMs – one for the central region jets and the other for the forward jets.
- There are some problems with the Jet CMM G-link readout firmware, for which Ian has been consulted.
- The construction of the new power bus-bar system for the Processor Backplanes is almost complete. It will be mounted on the new Wiener VME64x crate and mechanical demonstrator "dummy" Backplane, currently at RAL, which will be sent to Stockholm after Easter.

Next Phone Conference – Friday 23rd April 2004 at 10:00 (UK), 11:00 (Germany, Sweden)

Tony Gillman