Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 9th December 2004

Birmingham: **Stephen Hillier, Richard Staley, Dimitrios Typaldos, Pete Watkins**

Heidelberg: **Ralf Achenbach, Florian Föhlisch, Paul Hanke, Karlheinz Meier, Pavel Meshkov, Klaus Schmitt, Hans-Christian Schultz-Coulon**

Mainz: **Stefan Rieke, Uli Schäfer**

QMUL: **Eric Eisenhandler***

RAL: **Bruce Barnett, Norman Gee, Tony Gillman, Viraj Perera, Weiming Qian, Dave Sankey**

**at RAL*

1. Birmingham

- There has been a recurrence of the CPM-related VME problem first observed in January 2004, whereby one particular CPM (#4) occasionally generated an erroneous DTACK when a different module in the crate was addressed. In January, after some studies the problem had disappeared, but it had reappeared during the JEM FIO tests at RAL last week. Unfortunately, the effect could not be reproduced with the same modules in the Birmingham rig (although only one CMM was being used). To ensure identical conditions, these tests will be repeated in Birmingham next Monday, and if the effect is still absent then Richard and Gilles will study it in the RAL rig.
- The LVDS Source Module (LSM) and CPM v1.9 boards are ready for assembly, and completed modules should be delivered to RAL on schedule on 20th December.

2. Heidelberg

- The serial testing of the PPr ASIC wafers is well under way. The test processes, including the software, all appear very stable and the results are reproducible. Of the batch of 20 wafers delivered from AMS via the Fraunhofer Institute, 14 have been fully tested so far, at a rate of four hours per wafer. The overall yield to date is 55%, which is sufficiently high to provide enough dies for the PPr system.
- However, two worrying problem have been observed on some wafers:
    a) The failed dies are clustered into discrete groups, with between 10 and 20 dies in a cluster
    b) Patches of discoloration are seen, which seem to show damage to the passivation layer, and also dust deposits
- The good-die yield from wafer to wafer shows a very large spread, from 40% to 70%.
- These observations, which suggest a fabrication problem, have been fed back to the wafer manufacturers for comment.
- A second batch of wafers, to replace the original damaged batch, is due to be delivered to KIP next week.
- A statistical study of the analogue measurements on all accepted dies is being made, using the collated data from all the ASIC wafer tests stored in Pavel's database. So far, the evidence suggests that the parameter spread is very small, e.g. the distribution of currents drawn by good dies has a mean value of 321.5mA, with an rms of 3mA.
- Stress testing of some of the MCMs, involving temperature cycling and vibration tests using a loudspeaker, has been continuing, and a few devices have been subjected to operation at 120 degrees Celsius. One of the silicone gel-filled MCMs did fail under these conditions, with a bond wire going open-circuit. However, the two glob-topped MCMs both passed these tests satisfactorily.

- Arrangements are being made with Philippe Farthouat for the ASIC/MCM PRR to be held before the end of January 2005. Paperwork is being prepared so that the necessary contracts can be placed with two companies for substrate manufacture and assembly, once the PRR has been completed.
- Tests of the PPM have been continuing, with Pavel working on the software.
- A decision must be made very soon for when the next visit should be made to the RAL Slice Test rig. If possible, early in January 2005 would be good.

3. Mainz

- The full JEM FIO tests were successfully completed last week at RAL. The FIO mapping was not exactly as expected, because of firmware, but this was corrected by software to enable the FIO connectivity to be verified across the entire 16-slot crate space.
- Three of the four JEMs are working correctly in Mainz, but the fourth module continues to have configuration problems. Xilinx have been approached for help, but a solution has not yet been found.

4. RAL

- Tests of the 9U ROD have been continuing very successfully, and eight of the input links have been checked so far by feeding groups of four – supplying one Input FPGA – from a DSS. Via the Data Switch, an S-link then feeds the processed data back to a DSS for comparison. Some minor firmware mapping problems were seen but have been corrected. The remaining links still have to be checked in this way, and if successful a second (and possibly third) board will be assembled. Hopefully, the order can be placed before the end of the year.
- The decision had been made to use a larger (pin/footprint-compatible) FPGA for the Data Switch, at a cost of about £300 per device. If the lead-time to procure these devices is not too long, this will be fitted to the second board. These larger devices will definitely be used for the final production modules.
- The PRR for the CMM will be arranged to be held in January 2005. Philippe Farthouat's advice on some of the details – panel membership, documentation, etc – will be sought. One of the remaining important tests is to operate a pair of CMMs between crates, for which SCSI data cables of realistic (ATLAS) lengths (3m) are needed.
- The FDR for the Processor Backplane had been held on Monday 6th December at RAL. The outcome was successful, with no major changes being requested. Several mechanical issues relating to the Backplane-Crate interaction had been discussed, but solutions to all the problem areas had been found. A report on the conclusions and recommendations will be circulated for approval by the reviewers next week, and this will be entered into EDMS in due course.

Next Phone Conference – Thursday 13th January 2005 at 10:00 (UK), 11:00 (Germany, Sweden)

A very merry Christmas and a happy (and successful) New Year to all

Tony Gillman