Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 12th August 2004

Birmingham: **Steve Hillier, Jürgen Thomas, Dimitrios Typaldos**

Heidelberg: **Ralf Achenbach, Eike-Erik Kluge, Kambiz Mahboubi, Karlheinz Meier, Frederik Rühr**

Mainz: **Stefan Rieke, Uli Schäfer, Gernot Weber**

QMUL: **Eric Eisenhandler***

RAL: **Ian Brawn, Norman Gee, Tony Gillman, Viraj Perera, Weiming Qian**

Stockholm: **Christian Bohm, Sten Hellman, Attila Hidvégi, Sam Silverstein**

***** *at RAL*

1. Birmingham

As Richard was unable to attend, Tony reported the following points on his behalf:

- The schematics for the LVDS Source Module (LSM) are complete and available in pdf form on Richard's web pages, together with a specification document, at:

  http://www.ep.ph.bham.ac.uk/user/staley/LSM/

  The Cadence design files are also now ready for the RAL Drawing Office to start layout work.

- The CPM will undergo another design iteration to incorporate solutions to the problem areas already identified. All information for this revision will be prepared during August, and the schematics updated accordingly for submission to the RAL Drawing Office for layout during September. The major changes are as follows:

  - For the FIO signal layout, the 'envelope' of track lengths, and the number of vias, will be reduced to minimise the spread of transmission delays and improve signal quality. Certain routes are obvious candidates for this, and about 30 tracks are involved.

  - The PLLs will be replaced by Cypress CY7B9950 parts, which have a higher loop bandwidth but lower 'absolute' jitter than the current parts. This is important for PLLs connected in parallel.

  - For cost reasons, the dual optical transmitter devices used for the ROI and DAQ readout will be replaced by a pair of transceivers, and electrical outputs will be removed entirely. Uli suggested the use of Small Form-Factor Pluggable (SFP) devices, as used on the ROBINs. With unknown laser lifetimes, having replaceable lasers may be very useful and will be investigated further.

  - The ROC and G-link circuits will have the option to use the onboard 40 MHz crystal oscillator in addition to the TTC-derived clock.

  - The CAN microcontroller circuit will be modified to conform to the proposed common design from Adam.

  - The VME-- specification will be modified to include 3.3V signals, although this will not involve any design changes to the CPM.

  - Steve noted that Gilles' and Weiming's solution to the CPM-ROD G-link instabilities, involving modified grounding links to the G-link receiver chip on the latest G-link CMC cards, may not be the end of the story. Although Weiming had observed stable link behaviour over a period of 70 minutes, Bruce had observed other confusing link behaviour at CERN, inconsistent with this explanation, so it is unclear whether the cause of the problem is fully understood. However, it is essential that a solid solution is implemented before the September/October test-beam run.

2. Heidelberg

- Two of the three new PPM modules have been debugged by Klaus, and are now fully working. Some minor bugs were discovered, fixed and documented, and he will debug the third module once he returns from vacation.
- The re-designed LVDS Cable Driver (LCD) PCB cards are now out for manufacture, and should be ready for manual assembly in about three weeks.
- To equip the second PPM module for use at the test-beam, Klaus will modify another LCD card of the original design.
- Both PPMs will be brought to RAL for the integration week of August 23rd.
- The proposed PPM-JEM integration visit to Mainz is cancelled, as a mutually convenient date cannot be found. Instead, these tests can be done at RAL ~Monday 23rd August before the Mainz people return home.
- The ASIC wafer test setup continues to be developed, using the original ASIC wafers to optimize the needle probe parameters.
- The next batch of MCMs will be produced very soon. 61 devices will be assembled, using FR4 substrates and the new ASIC dies. There will be a visit to the assembly company in September to check on the test and repair procedures.
- The ASIC/MCM PRR documentation is in preparation, with a draft available on the web.
- Frederik has discovered that the TileCal and LAr calorimeter modules at the test-beam are displaced relatively by half a trigger-tower in ϕ, but this should not cause any problems.

3. Mainz

- On the first JEM (1.0), three of the four Input daughter-cards have now developed dead channels. This is believed to be caused by the delay between PCB manufacture and assembly.
- The three new JEM modules and 16 new Input daughter-cards (to equip all four JEMs, including replacement of the original faulty daughter-cards) are currently being manufactured. They are expected back at Mainz ~now, and will be tested once Bruno returns from vacation.
- One 16-bit G-link transmitter chip on a daughter-card has been tested and is working. It will be brought to RAL for the next integration week, together with the 20-bit version. However, to minimise ROD firmware changes, only the 20-bit version will be used at the test-beam. Kambiz asked whether the PPM might also use the 16-bit G-link transmitter chip, but the current data formats may not permit this.
- Stefan has been developing the online software, and tying it to the modules database. He can mask off the dead channels on the Input daughter-cards.
- Gernot has been writing firmware for the CAN microcontroller on the JEM. He can measure the temperatures on all of the module FPGAs (the Input daughter-card FPGAs run at the highest temperatures). It is planned to operate the JEM CAN system at the test-beam. At present, the CAN data are output directly from the Backplane bus, but eventually they will be interfaced via the TCM.

4. RAL

- The first two optical G-link receiver CMC cards have been tested successfully, and testing of the remaining four cards should be completed within the next few days. (N.B. late news – Adam reports that all the cards – transmitters and receivers - are now working correctly and are available for use).
- The 9U electrical → optical converter module is being manufactured and should be back at RAL on 18th August.

- The 9U ROD module should be back from manufacture on 13th August. (N.B. late news – delayed until 18th August).
- Adam has written a draft proposal for standardisation of CAN microcontroller pinouts, which will be circulated to the collaboration.
- The schematics changes for the re-designed TCM and VMM modules will be started next week. Updating the specifications documents has also started, ready for an internal FDR in the next few weeks.
- The new TCM will distribute the backplane TTC clocks via low-voltage PECL.
- Ian reported that the 9U ROD firmware was progressing well, and will be sufficient for the imminent arrival of the hardware.
- Synchronicity licences are now available for all the ROD designers, although only Ian and James are currently active users. Some access problems are being addressed before its use is adopted generally.
- Implementation of requested CMM firmware changes is stalled due to the absence of a Processor crate in the Test Lab (the crate used originally was shipped to the CERN test-beam last month). It may be necessary to bring the PC running LabView across temporarily to the Trigger Lab in R1.
- Some of the components (FPGAs) for the new CPM design have long delivery lead-times, so will need to be ordered quite soon. We should explore the possibility of salvaging the large (expensive) CP FPGAs from the five original CPMs, once they are no longer needed, and getting them re-balled, although that may cause problems because of the conditions imposed on component procurement by the "one-stop shop" companies.
- The latest "hot potato" to be raised concern the mixture of numbering systems employed throughout the trigger: should labelling start from 0 or from 1? At present, both are found in different places. It was felt that uniform consistency should be imposed…

5. Stockholm

- Attila has already circulated a short report of progress with the jet-FPGA at RAL.
- There has been progress with the electro-mechanical work on the Wiener 9U Processor crate, in particular with cable strain relief hardware, the power bus-bar system and the provision of Backplane stiffening ribs. The CMM Rear Transition Modules (RTMs) will also need some form of strain relief, so Viraj will send Sam the relevant Gerber files for these cards.
- Sam has provided and tested a small PCB for attachment of the power supply sense wires to the power distribution bus-bars. He has also measured the δV drop along the individual power feed cables to the module slot connectors, and finds a δV of 60mV when supplying 24A to a single slot. This corresponds to a resistance of ~1.3mΩ for each of the power and ground cables. It was noted that the Concurrent SBC fails if its supply voltage falls by more than 250mV, but as it only draws ~10A the voltage drop should be ~25mV.
- Some Backplane measurements must still be made with the JEM FIO signals, but as these will require two JEMs they cannot be carried out during the next integration week at RAL.
- Trials of the procedures for replacing Backplane connector pins must also be made.
- The Backplane FDR (internal) is scheduled for September 2004.

Next Phone Conference – Thursday 26th August 2004 at 10:00 (UK), 11:00 (Germany, Sweden)

Tony Gillman