# Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 16th January 2004

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| **Birmingham:** | **Steve Hillier, Gilles Mahout** |
| **Heidelberg:** | **Ralf Achenbach, Florian Föhlisch, Eike-Erik Kluge, Victor Lendermann, Kambiz Mahboubi, Karlheinz Meier, Pavel Meshkov, Frederik Rühr, Klaus Schmitt** |
| **Mainz:** | **Cano Ay, Stefan Rieke, Uli Schaefer** |
| **QMUL:** | **Juergen Thomas** |
| **RAL:** | **Bruce Barnett, Ian Brawn, Tony Gillman, Viraj Perera, Weiming Qian** |
| **Stockholm:** | **Attila Hidvegi, Sam Silverstein** |

## *1. Birmingham*

- Operating three CPMs in adjacent slots, occasional loss of G-link lock is seen, believed to be caused by excessive jitter on the TTC clock. Some TTCdec cards exhibit much more clock jitter than others, but the p-p value can approach 1 nsec.
- The VME problem observed with CPM5 at RAL (spurious DTACK response, with abnormal DS-DTACK delay) is not observed in the Birmingham test rig, with three CPMs, CMM and TCM in the crate.

## *2. Heidelberg*

Karlheinz noted that Paul is making good progress, and had already visited KIP.

- Redesign of some of the PPM digital circuitry (VME interfacing, FPGA configuration, Flash RAM access) is complete, and a lot of work has been done on the layout which is now almost finished.
- The analogue routing (manual) is finished, but the auto-routing of the digital sections needs more iteration(s) – so far, eight runs have been made. The design has ~6,000 vias and ~2,400 components.
- Submission to Wurth is expected next week, with a ten-day turnaround.
- The first four PCBs will be assembled in small stages in-house at KIP – hopefully by the end of January. Further (production) modules will be assembled by outside manufacturers.
- Tests of the LAr Receiver module, using the video DAC system, will take place at KIP at the end of January, when Vladimir Savinov will visit for three days. The module, together with its USB interface and software, is being delivered ~now.
- The layout of the re-designed AnIn (analogue input card), using single-channel amplifier chips, is complete.
- The re-designed PPrASIC has now been submitted for fabrication, and the wafers are scheduled for return in about eight weeks.
- Kambiz is working on the coding for the ReMFPGA.
- The KIP trigger web pages are being updated, and will include registration details for the Collaboration Meeting in March.
- Manufacture of the MCM substrate continues to give problems. A new batch of substrates has been received from Wurth, but containing only 30 devices from the total order of 100, which suggests a low yield. More information will be obtained from the company. The separate order of 100 substrates from the Swiss company is expected to arrive on 9th February.
- Pavel has set up a burn-in test facility for the assembled MCMs, which will provide an accelerated temperature cycling and vibration environment.
- By the end of January, Pavel will also prepare the necessary software to test the PPrASIC and MCM at three separate stages of assembly. Automated test software will be required for production.

- Florian is working on several aspects of the DAQ software, and will soon visit Cano in Mainz. He has now finished reworking the PPM register map.

### *3. Mainz*

- The G-links on the JEM1 will be located on daughter-cards, which will also carry the Stratos optical transmitters. The final PCB layout will be submitted to Rohde & Schwarz for manufacture next week.
- The RAL integration tests have successfully demonstrated the transfer of data via the backplane from two JEMs to two CMMs. Correct energy summing (and appropriate cancellation to zero for opposing quadrant data) was observed.
- DAQ/RoI data transmission to RODs is suffering from G-link hardware problems.

Details of the integration tests can be found in the AT1INTEG summary mailings from Bruce (16/01/04).

### *4. QMUL*

Details of the CMM tests can be found in the AT1INTEG mailing from Murrough (15/01/04).

### *5. RAL*

- The schematics for the new 9U ROD design should be ready for checking next week, and it is hoped that it will be sent to the Drawing Office for layout by the end of January.

### *6. Stockholm*

- Uli and Attila will discuss updating firmware to be compatible with the JEM.
- The Geographical Addressing problem with the Processor Crate Backplane/switch could be fixed by defining all lines to be active-high, and setting the carte switch to N = (7-crate no).
- Work is continuing on defining a cable support scheme for the rear LVDS cables, and also for improving the power supply bus system on future crates.
- A tool to replace broken backplane connector pins will be ordered.
- If available, multi-length connector pins would be very desirable for the production crate backplanes.

**Next Phone Conference – 30th January 2004 at 10:00 (UK), 11:00 (Germany, Sweden)**

***Tony Gillman***