Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 17th June 2004

Birmingham: **Gilles Mahout, Richard Staley, Jürgen Thomas, Dimitrios Typaldos, Pete Watkins**

Heidelberg: **Ralf Achenbach, Florian Föhlisch, Christoph Geweniger, Paul Hanke, Eike-Erik Kluge, Kambiz Mahboubi, Karlheinz Meier, Pavel Meshkov, Frederik Rühr, Klaus Schmitt, Hans-Christian Schultz-Coulon**

Mainz: **Uli Schäfer**

QMUL: **Eric Eisenhandler, Murrough Landon**

RAL: **Bruce Barnett, Norman Gee, Tony Gillman, Viraj Perera, Weiming Qian**

Stockholm: **Attila Hidvégi**

1. Birmingham

- Gilles reported that the extensive work carried out on the CP FPGA firmware has been very successful, and the new CPMs (CPM1.5) now exhibit a clean 1 nsec timing window for all 160 Mbit/s data (onboard and backplane), checking for parity errors over periods of ~1 second. This timing window may improve further with the addition of a low-jitter PLL.
- These measurements will be repeated with long (overnight) runs in order to look for bit-error rates per input pin at the 10^{-13} level. Studies will also be made of the effects of elevated temperatures.
- At present, the CP FPGA has a utilisation factor of ~96%, but there is scope to reduce this by removing some redundant functional blocks. It is expected that the latency should also reduce by at least 1 clock tick.
- The performance of the backplane has been studied intensively with Sam over the last three days.. Three CPMs in adjacent slots were used, with the central module fully populated with LVDS link data from a set of DSS modules, and measurements of ground bounce, crosstalk and the effect of VME activity all demonstrated no adverse effects.
- All 16 JEM slots were used to verify that hit data were transferred correctly across the backplane to the RH crate CMM.

2. Heidelberg

- Ralf and Pavel have been testing the first wafer of the new PPr ASICs, using the wafer prober system with the full range of automatic tests that have been developed at KIP. The results so far are extremely encouraging. 154 dies from the total of 180 on the wafer have so far been tested, and the yield of good devices is 60-70%, where 60% was the predicted figure.
- Authorisation will now be given for the full ASIC production of 50 wafers, which will be completed in about two months. Automatic testing will take about half a day per wafer.
- The new MCM FR4 substrates have all successfully passed the bond strength pull tests, so authorization for their full production can now be given.
- The first 60 MCM lids will be machined from solid brass in the KIP workshops.
- The PRR for the MCM, fully assembled with all tested components including the PPR ASIC, will be held in Heidelberg in July, based upon the successful demonstration of a small number (~10) of working devices.

- The first PPM, which was at CERN last week for the test-beam studies, is now back at KIP for further studies. The next three PPMs are ready for assembly next week at a company which has a proven track record for successful board assembly.
- The LVDS Cable Driver (LCD) board proved to be very difficult to lay out, partly because of the numerous controlled impedance differential traces, so hand-routing was found necessary. This was very time-consuming, and so the pcb manufacture was only started last week. With a 10-day turnaround time, the first bare boards will be back at KIP next week.
- Assembly of the LCD boards will be done manually at KIP, but the timescale is such that the LVDS integration tests in Mainz, first with a JEM and then with a CPM, will not now take place before the Stockholm collaboration meeting. Allowing for assembly and bench testing, these integration tests may now take place later in July at Mainz, or possibly at RAL as the final part of the Slice Test integration work.
- All ten of the 9U PPr crates, which have already been delivered to KIP from Wiener, will undergo testing.
- It seems that the delivery of the main 9U ROD crates, which was scheduled for November, has been delayed until February 2005. This should be followed up urgently, as we have no other crates with power supplies providing 48V, as required by the 9U ROD modules.
- Paul reported on the successful outcome of their visit to the ATLAS test-beam, where the first PPM was integrated with TileCal trigger signals via the calo-muon trigger Patch-Panel and a LAr (TileCal) receiver module. Using the TileCal charge-injection calibration pulser system, they transferred signal pulses right through the analogue chain and recorded the digitised versions in the PPr ASIC memories. The external BCID discriminator outputs were "OR"ed to provide a simple L1A trigger for transferring the digitized data from scrolling memories to the derandomiser buffers and reading them out. For comparison, DSO traces were captured of the analogue signals before digitisation. LAr signals were unfortunately not available, but with the help of Paulo Da Silva (Rio) several amplitudes of TileCal calibration signals were successfully digitized and read out. A detailed report of the work will be available soon.
- Florian presented a summary of his recent work on the DAQ software. Further details were reported at the Software phone conference on 14th June, the minutes of which can be found at http://hepwww.ph.qmul.ac.uk/l1calo/sweb/meetings/2004/mins-06-14.html.

3. Mainz

- The first JEM1.0 module was successfully integrated with the CMM and ROD modules at RAL last week. Detailed summaries of the work have already been sent out by Bruce and Jürgen to the Integration mailing list, so only a brief summary is given here.

  Slice data (1, 3 and 5 slices) from a DSS were successfully processed through the JEM1.0 to the ROD in agreement with simulation. The minimum 5-tick L1A separation operated correctly.

  Running data into two energy-sum CMMs also produced agreement with simulation. However, readout of CMMs via the ROS at a 65 kHz trigger rate produced a 1% error rate with 1/503 sampling, which needs further study.

  An overnight run with JEM readout at 46 kHz (4 million events processed) was error-free.

  The TTC clock jitter (measured using G-link fill-frames) was very low, even with a L1A rate of 100 kHz.

  The new jet algorithm was operated, with the JEM1.0 fed with 16 LVDS inputs and sending jet data to the RH CMM (running CP merger firmware). Readout was initiated from the CMM through the ROD and S-Link sink and compared with the simulation.

Unfortunately, although jet data were sent to the backplane problems were seen with unreliable threshold register settings, which produced unexpected jet multiplicities.

- The module is operating once more in Mainz, so that the jet algorithm problems can be further studied. Tests of the CANbus and flash memory configurators are still to be completed.
- All remaining tests should be finished quite soon, and the next three modules will then be assembled.
- The next batch of Input daughter-cards will be ordered next week and should be available by the end of July.
- Uli suggests that replacement of the dual optical transmitter modules that we are currently planning to use on the CPMs, JEMs and CMMs by a pair of optical transceiver modules would save significant costs when we move into production. This will be looked into further.

4. RAL

- The pcb layout of the 9U ROD module is now complete, and quotes are being sought for manufacture. Delivery of two components is still outstanding – memory chips and the 48V DC-DC converter module. Three pcbs will be produced, but initially only one will be assembled.
- There has been good progress with the ROD firmware. The Synchronicity archiving tool has at last been made available for Ian to use as the code develops. Weiming has been working on some of the 6U ROD firmware, and this code should also be put into Synchronicity as soon as possible.
- The long list of comments on the latest ROD specifications is being compiled by Eric. Fortunately, none of them so far involves any changes to the schematics or to the pcb layout, as it is expected that the design will be sent for manufacture next week.
- With the recent decision to change all G-link signal paths to optical for reliability, it has been decided to re-design the G-link transmitter and receiver CMC daughter-cards for the DSS and 6U ROD modules to incorporate optical transmitter and receiver modules in place of electrical sockets. The first of these new pcb designs is now being laid out.
- Paul asked how the PPM G-link readout data links could be checked. The DSS with G-link receiver daughter-cards has been the usual procedure for testing slice and RoI data links from other modules, so one would be provided when needed.

5. Stockholm

- Attila commented that the cause of the problems seen at RAL with the JEM1.0 configured with the jet firmware is still unknown. It seems to work correctly in Mainz. Presumably, the tests should be repeated in the RAL system environment so that the problems can be investigated further.

Next Phone Conference – Thursday 15th July 2004 at 10:00 (UK), 11:00 (Germany, Sweden)

Tony Gillman