ATLAS Level-1 Calorimeter Trigger Hardware Phone Conference Notes
19 May 2004

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Birmingham

- Much progress has been made with the new CPM 1.5. The mystery of pins not correctly receiving data has been understood to be a firmware problem involving a clock and a DLL; it was only by luck that this was not present on the previous CPM 1.0. The problem is fixed.
- The idea of using two clocks to get the backplane data in time does not work because of a lack of resources in the CP FPGA, but a workaround is to use one clock for on-board and some of the backplane data, and another clock for the remaining backplane data. This also requires some phase reversals of signals in the Serialiser with firmware modifications. All this has not been easy to understand or do, but is now working in scanpath mode; the algorithm mode is now being worked on. The timing window for backplane signals looks like 2 ns by eye (it was 1 ns) so full soak tests should yield better than 1 ns. If the algorithm mode behaves similarly, this should be sufficient for slice tests; in the final CPM version the track lengths will be corrected and hopefully fix the timing in a better way.
- The LVDS Source Module (LSM) design is progressing well, schematics are nearly done.

Heidelberg

- The final stage of testing the new ASICs, namely the on-chip histogramming, is now starting.
- The PPM hardware is still being tested as new firmware is developed and debugged. Offers have been received for assembling three additional PPMs, and if all goes well the PCBs will be sent out on 28 May and come back assembled two weeks later.
- Some work on the online simulation of the PPM has been completed at Birmingham.
- The new analogue input daughter card (with single-channel chips) is now tested (a few minor things were fixed) and ready to go out for production. The LVDS output daughter card is now laid out and also goes out to be built on 28 May.
- The 16-fold video card for testing analogue inputs is now finished.
- The next test will be with calorimeter signals and receivers, in the test-beam starting 7 June.
- Work continues on the firmware. Emphasis at present is on VME access for the beam test; this also allows testing of PCB tracks on the boards, which is essential before assembling more PPMs. A current problem is correct operation of the TTCrx, which needs ‘offline’ discussion. Firmware for DAQ readout is clearly needed for the slice test and is planned, but at present the priority must be with the things mentioned above.

Mainz

- The new G-link daughter card (supplied with the electrical option) has been tested at Mainz as far as possible; soak tests will come later.

- Under abnormal conditions, the input processors on JEM 1 hang — this does not happen in normal operation. It cannot be reset when this happens; work is concentrating on the CPLD used for VME access. Further testing, e.g. at RAL, will proceed when this is fixed.
- The JEM 1 will be tested with combined energy and jet firmware, for both the realtime path and readout, as soon as work on the energy side has allowed obvious problems to be cleared. It will probably be at least 2–3 weeks before it makes sense to test it at RAL.

RAL

- The 9U ROD track layout is now done; after some manual 'cleanup' and laying out of power planes it can be sent for manufacture, around 28 May. Work is being done on firmware for the Input FPGA FIFOs and handling of neutral data format, with the VME map and TTC broadcast mode soon. The S-Link rear transition module is designed and quotations for building it are being sought.
- The 6U ROD firmware is being updated to handle the new version 2.4 of the S-Link format, as required for the test-beam.
- Modifications are needed to CMM energy firmware and will be done soon.
- Construction of optical versions of the PPM G-Link rear transition module awaits successful testing of the electrical version.

Stockholm

- The jet FPGA firmware is now written, and FCAL handling has also been added for the appropriate modules. The input mapping needs to be modified. Tests will be done at Mainz. This firmware also has to be documented and added to JEM documentation.
- A phone conference to summarise what has been done and what needs to be done in the Processor Backplane test programme will be held on Friday 28 May. Note that the Backplane falls below the PRR 'threshold' cost, so only an internal final review is required. (This is also true of the TCM and the VMM.)
- The ATLAS-standard processor crate at RAL has been shipped to Stockholm to allow checks of the new busbar hardware design.
- Web information on the June/July Joint Meeting in Stockholm will be posted in the next few days.

General

- There was some discussion about tests of the LVDS interface from the PPM to both JEM 1 and the CPM. The most obvious solution is to do that as soon as possible at Mainz, starting with the JEM and then proceeding to the CPM, unless there are unexpected problems with the schedule.
- A new plan of what to take to the test-beam, with the aim of leaving enough at the home labs to continue testing, as well as a new schedule based on the current situation, are being worked on. These ideas will be available soon, and can be further discussed at Stockholm (though we will need to have decided on a lot of it by then.)

Next phone conference: Thursday, 3 June 2004 at 10:00 (UK), 11:00 (Germany, Sweden)