Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference –23rd April 2004

Birmingham: **Richard Staley, Pete Watkins**

Heidelberg: **Ralf Achenbach, Florian Föhlisch, Paul Hanke, Kambiz Mahboubi, Karlheinz Meier, Pavel Meshkov, Frederik Rühr**

Mainz: **Uli Schaefer**

QMUL: **Eric Eisenhandler**

RAL: **Bruce Barnett, Ian Brawn, Tony Gillman, Viraj Perera**

Stockholm: **Sten Hellman**

1. Birmingham

- Commissioning of the two CPM1.5 modules has continued to progress well
- All VME accesses are working correctly, FPGA configuration data can be downloaded and the Serialiser, CP and ROC FPGAs can all be configured correctly.
- All four LVDS deserialisers checked so far lock correctly.
- For real-time data, on-board scans show timing windows similar to those on the previous CPMs.
- Backplane data from the same two pins on three CP FPGAs fails to be captured correctly, which is very suspicious. When diagnostic firmware was used to route these pins to test-points for ‘scope observation, the signals appeared normal, so the data are at least connected. More investigation is needed.
- Gilles has modified the CP FPGA firmware to make use of the second backplane data strobe to improve the timing margins. It will need some slight modifications to the CPM pcb to re-route the VME strobe before testing at Birmingham next week.
- Tamsin has modified the CPM Serialiser firmware to fix the old PPr ASIC "odd parity" bug. Testing it will require coordination of hardware, firmware and simulation code changes, which will hopefully take place in Birmingham next week.
- After a lot of detective work, Richard has calculated that by re-routing a maximum of 31 CPM backplane data traces (currently, 12 are too long, and 19 too short compared to their other bus members), propagation delays could be sufficiently equalized to increase the data timing window by as much as 1 nsec (assuming also the use of the two available backplane data strobes).

2. Heidelberg

- Frederik spent some time looking at the ATLAS Test-Beam set-up whilst at CERN this week. A plan is needed to define where the LAr Receiver(s) and the PPM setups are to be located - upper-level or lower-level counting rooms.
- Unfortunately, the Test-Beam schedule has been delayed by at least one week because of a water leak in the PS Booster, which implies that the 25 nsec run probably won’t happen until June 15th. However, the integration of the PPM with the LAr Receiver will still go ahead on the original timescale, taking asynchronous data. The hardware will be left at CERN for a possible return visit for the delayed 25 nsec run.
- For the new PPM, Kambiz reported that 30-40% of the ReM FPGA firmware has been written and simulated, and all the VME protocols and access have been tested.
- About 10-20% of the PPM motherboard functionality has been tested, including the TTC clocks, although the I2C interfacing has not yet been tried.

- Software is needed to access the PPr ASIC via its serial interface. Pavel is continuing to develop the test software.
- Florian will work with Murrough at QMUL next week on the PPM database.
- Ralf is collating the data from the MCM bonding tests, which were performed with the polyimide-surface substrates from Wurth and Dyconnex..
- The new batch of MCM substrates using FR4 material should be delivered early in May.
- A new date for the ASIC/MCM PRR will be defined only after the new substrates have been confirmed to exhibit good bond strengths and good yield.
- The remaining three PPM pcbs will be assembled at two different companies. One has already been visited, and the other will be visited next week. Quotes for assembly will then be obtained from both companies.
- Tests to establish successful interfacing of a PPM with both a JEM1 and a CPM1.5 will be done in Mainz in early June, before the ATLAS Test-Beam run(s). These tests will use the full 15m LVDS cable assemblies, with pre-compensation.

3. Mainz

- The first JEM1 has been fully-populated with all daughter-cards.
- Unfortunately, during manual assembly of the G-link daughter-card some shorts were created on the 0.5mm pitch surface-mount connectors, leading to blown fuses on module power-up, and destruction of the G-link daughter-card. A new card will be assembled (non-manually) over the next week or so, and (assuming that the rest of the module is undamaged) testing can continue.
- The firmware for the ROC is complete and will be tested next week.
- I2C control of the TTCrx chip works correctly.
- Channel mapping into the Input FPGAs has some errors, which need to be corrected in the firmware.

4. RAL

- Viraj showed the UK people the layout of the 9U ROD, whose component placement should be finalised in the next couple of days. Some trace routing has already been done, and the remainder should be finished within two weeks.
- Ian and Adam have begun to write the firmware, and will be joined by James when he returns on May 4th.
- Two modules (pcb and assembly) will be manufactured initially, at a different company from that used for the CPMs, in order to widen the pool. The modules should be completed by early June.
- The Wiener VME64x crate at RAL lacks the necessary 48V power module to operate the ROD, so as a temporary solution a bench power supply will be used, feeding the 48V bussed power into the crate via a card plugged into a spare J1 slot. When the first new Wiener ROD crate is delivered to RAL some time in June, it will already be equipped with a 48V module, so the current crate/PSU will then be returned to Wiener (via CERN) for the necessary modifications.
- Ian reported that the I2C interface on the CMM has now been debugged. An error was discovered on the schematics where a pull-up resistor had been omitted from an open collector device, thereby preventing a strobe signal being generated. Three modules now work correctly, and the other two will be fixed soon.

- The firmware controlling the I2C access had a bug causing unreliable behaviour, which has now been fixed.
- One CMM had a bad connection to an FPGA, which could not be repaired, so the firmware was modified to re-route the signal to another pin. At present, this means that two different firmware versions are needed.

5. Stockholm

- Attila has now completed the Jet FPGA firmware. There remain some small problems concerned with pin configurations which he will discuss with Uli.

Next Phone Conference – Thursday 6th May 2004 at 10:00 (UK), 11:00 (Germany, Sweden)

Tony Gillman