Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 26th March 2004

Birmingham: **John Garvey*, Steve Hillier, Gilles Mahout, Richard Staley, Dimitrios Typaldos**

Heidelberg: **Ralf Achenbach, Florian Föhlisch, Christoph Geweniger, Kambiz Mahboubi, Pavel Meshkov, Frederik Rühr, Klaus Schmitt**

Mainz: **Cano Ay, Uli Schaefer**

QMUL: **Eric Eisenhandler***

RAL: **Bruce Barnett, Ian Brawn, Norman Gee, Tony Gillman, Weiming Qian**

Stockholm: **Sten Hellman, Sam Silverstein**

at RAL

1. *Birmingham*

- The first two CPM1.5 modules were delivered two weeks ago, and both have now successfully passed their JTAG tests.
- The first module has been under test only since Wednesday All LVDS deserialisers lock correctly, and receive apparently correct data.
- One of the PLLs had to be changed for a different part.
- The DAQ readout path works properly, with no detectable jitter from the new TTCdec card, although the offset has apparently moved by one clock tick.
- The CP FPGA timing windows are not as wide as had been expected. The on-board scanned data windows measure 3.5 nsec by eye (low statistics), but only 2.5 nsec when measured quantitatively with high statistics using the parity bit flag. However, when fed from a second (old) CPM, the timing window reduces to ~1.5 nsec, which is not significantly better than measured on the old modules. Also, there is a large (2 nsec) Δt between data from different Serialisers feeding a single CP FPGA, which could be due to unexpectedly large differences in trace lengths (corresponding to Δl of ~40 cm). The PCB routing data are being studied to understand the cause of the problem, and the second CPM1.5 will be measured for confirmation.
- On solution might be to use both of the two available data strobe clocks for latching the Backplane data into the CP FPGAs (at present, only one is used). The phase of each can be independently adjusted in 700 psec steps, but the CP FPGA firmware would need modification to enable some inputs to be strobed with this second clock. In general, each CP FPGA would require its own combination of clocks and associated data, and hence a unique firmware load. In the worst case, this would mean the provision of eight configuration files per CPM.
- Tuning the timing of data from the Serialisers might also help, but this may create problems for capturing the on-board data.
- The quality of the data waveforms looks good along the daisy-chained paths, implying good impedance control on the long traces.

2. *Heidelberg*

- People have been preparing for the Deutsche Physikalische Gesellschaft conference in Mainz next week.
- The first PPM continues to be tested. Klaus has changed the VME addressing from A24 to A32, and the VME CPLD has been loaded correctly via JTAG. The new TTCdec has been operated

successfully, but the MCMs have not yet been loaded. Problems with the power-up/power-down sequencing have been fixed. Kambiz has agreed the data format for the ReM FPGA firmware, which should be completed soon.

- The layout of the LVDS fanout daughter-cards for the PPM is ~90% complete, and its routing will be started next week. Its FPGA also requires some (relatively straightforward) firmware to be written before it can be used.
- This first PPM will hopefully be available for the Slice Tests in about two months from now.
- A few people recently visited Wurth to try to understand the low yield of MCM substrates (<5%?), and a further 15 substrates have since been delivered to KIP. It seems that the polyimide material used as substrate for the thick film process is effectively to uneven, so the remaining 55 devices (from the original order of 100) will be manufactured using "standard" FR4 (PCB) material, for delivery in May. It is claimed that all Wurth's customers using polyimide material have experienced similar problems.
- Dyconex have produced 280 substrates, of which 170 are classed as "good" devices, from which 100 have been delivered to KIP, but these still have to undergo bond pull tests, the results of which will be available by the end of next week.
- 5.5 wafers, plus 20 separate dies, of new PPr ASICs have been received at KIP.
- The limited number of tests on one die have so far been successful, including the confirmation that the parity bug has been corrected. However, the necessarily thorough test programme, with new tests to cover ~100% of the ASIC functionality, requires some further software, which will not be available for another 3-4 weeks.
- Florian has been working on the CERN drivers for the KIP custom in-crate processor, which is working properly in A24 mode. It has not yet been tested with actual online software.

3. Mainz

- The next three Input daughter-cards have suffered from soldering problems on assembly, possibly caused by the PCBs having been stored for more than six months after manufacture. An extra surface cleaning stage may be required.
- The first JEM1 cannot be boundary-scanned yet as the necessary tester is not currently available.
- The JEM1 firmware can be loaded correctly, and the Sum FPGA also configured via VME.

4. RAL

- PCB layout of the 9U ROD is progressing well, with placement and routing of the 'modules' almost complete. They will be imported into the rest of the board starting next Monday.
- James is entering the 9U ROD block diagram so that firmware designs can start soon.
- Ian and James will set up the Synchronicity tool next Monday, and the first meeting of the 9U ROD firmware designers will be arranged for the following week, when all the designers will meet to discuss work plans for firmware designs.
- Adam Davis will design the firmware for the VME FPGA and the Initialisation CPLD following the departure of Panagiotis.
- Adam has been working on the CANbus, together with Andrey. For this to be more efficient, we will buy a KVASER PCI CAN card for RAL so that tests can be made at both sites when problems arise.

- Tamsin has almost completed the parity bit correction for the Serialiser FPGA firmware, and the plan is to test this next week on a CPM fed with simulated data from a DSS.
- For the two possible extra CPMs, the XCV100Es (Serialiser) FPGAs will be ordered now, as they have a lead time of 12 weeks. Although the XCV1000E (CP) FPGA currently has a lead time of 4-5 weeks, this can rapidly worsen (e.g. in February the situation was the reverse!).
- There were concerns regarding the updating of design tools during the Slice/Beam tests, which could temporarily prevent urgent firmware changes. As updates for all the tools (Mentor Graphics and Xilinx) are under our control, this will not be a problem since we will avoid any updates during these periods.

5. Stockholm

- Attila has been looking at VME access to the Sum and Jet FPGAs. In order to free some I/O pins, he needs to multiplex the VME lines.
- Sam has been looking into the Jet CMM code for handling the F-CAL data. He will discuss this further with Norman and Ian.
- Sam has placed an order for the custom backplane connectors (with the long tails for LVDS cables).
- Three companies may be bidding for the final Backplane contract.
- A tool-kit for in-situ repair of broken Backplane connector pins is available, but at a high price and with a minimum order quantity of four kits. This may still be a viable option as such kits would be needed at several locations during ATLAS running.
- A Backplane Working Group has been formed to consider all aspects of this component (including a comprehensive test programme) before preparing for its FDR and PRR.

Next Phone Conference – Wednesday 7th April 2004 at 10:00 (UK), 11:00 (Germany, Sweden)

PLEASE NOTE CHANGE OF DAY TO *WEDNESDAY* (FOR THIS PHONE CONFERENCE ONLY), AS FRIDAY 9th APRIL IS A UK PUBLIC HOLIDAY (EASTER).

Tony Gillman