Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 26th August 2004

Birmingham: **Gilles Mahout, Tamsin Moye, Jürgen Thomas, Pete Watkins**

Heidelberg: **Ralf Achenbach, Florian Föhlisch, Paul Hanke, Eike-Erik Kluge, Kambiz Mahboubi*, Karlheinz Meier, Pavel Meshkov, Frederik Rühr**

QMUL: **Eric Eisenhandler***

RAL: **Bruce Barnett, Ian Brawn, Norman Gee, Tony Gillman, Weiming Qian**

Stockholm: **Christian Bohm, Sten Hellman, Attila Hidvégi, Sam Silverstein**

***** *at RAL*

1. Birmingham

- Richard has made a number of changes to the CPM schematics, in preparation for the next – and hopefully final – design iteration. One of the last remaining issues to be finalised is the CANbus architecture and choice of microcontroller, for which Adam has proposed a specific device. It is expected that the new design (provisionally known as CPM1.9) will go for PCB layout in September.
- With the reference clock in the ROD G-link receivers run at 40.00 MHz, clocking the G-link transmitters on the CPM1.0 and CPM1.5 modules at the 40.08 MHz LHC frequency (e.g. from the TTCex-sourced TTC clock) produces difficulty in establishing link lock. This is because the 0.2% Δf exceeds Agilent's recommended maximum deviation of 0.1%. Gilles has made some firmware change to the ROC to enable the G-link transmitters to be driven from the on-board 40.00 MHz crystal oscillator, and this will be tested when some small wiring changes have been made on a CPM1.5. The JEM1.0 can already operate its G-links reliably in this fully asynchronous mode, and it is intended that all other source modules (PPM, CPM and CMM) will also operate in this mode finally. However, at the test-beam, reading out the CMMs presents a potential problem, as the relatively simple CPM fix cannot be applied to the CMM. Ian's proposed firmware-based solution would require considerable time to implement with no guarantee of success. Changing the frequency of the G-link receiver reference clock in the CMM ROD to 40.08 MHz (using the custom QPLL crystals) is also possible, but again with considerable difficulty.

2. Heidelberg

- The batch of 61 MCM substrates is currently being assembled with ASICs and other components at Hasec. They are expected back at KIP this week and will be tested over the next few days. Any faulty devices will be returned to Hasec for reworking.
- The first six re-designed LVDS Cable Driver (LCD) PCBs have been received, and will be assembled in-house when Klaus returns from vacation. For the test-beam work, Klaus will modify and then assemble a second LCD of the original design to equip a second PPM.
- A new batch of 18 AnIn cards has also been received, for assembly by a commercial company.
- Procedures for the ASIC wafer tests are now generating fully reproducible results, after repeated re-testing.
- Paul noted that he has posted the draft documentation for the ASIC and MCM Production Readiness Review on the web. However, the date for the PRR itself will not be determined until a sensible number of MCMs of the latest design have been shown to work.
- Kambiz summarized the integration tests with the first PPM that had been taking place during the week at RAL. Several problems had been encountered, some of which were related to the ReMFPGA firmware. In particular, the Virtex-E FPGA had limited global clock distribution resources. Four or five variants of the firmware had been tried so far. As well as the real-time signals, the G-link data

outputs had also been looked at, initially using internally-generated test data from the G-links. The priority was first to sort out the real-time data path using Playback data into the JEM and the CPM before studying the readout path.

- To avoid adverse interaction between different parts of the firmware, Paul wondered whether certain working sections of the code could be frozen when other parts had been modified. Ian noted that this was in principle possible, by creating macros. However, Kambiz commented that in the case of the ReMFPGA firmware the restricted number of clock distribution resources made this very difficult. He noted that he has already removed the Des2 clock from the firmware, thereby freeing up one extra clock distribution resource. The addition of ChipScope to the design would be very valuable as a diagnostic tool, but this would require an extended. JTAG chain.

3. QMUL

- Eric noted that the Final Design Review of the CMM will be in CERN during the week beginning 20th September 2004. Eric will chair the review, and the following have agreed to act as reviewers:
  - Dave Charlton (Birmingham)
  - Tony Gillman (RAL)
  - Gilles Mahout (Birmingham)
  - Ralf Spiwoks (CERN)

  A second CERN person has been asked to act as a reviewer to represent TC, but is currently on vacation.

4. RAL

- Ian summarised the status of the firmware packages for the 9U ROD.
  - Input FPGA: The neutral format firmware is complete, but some further simulation is required.
  - Switch FPGA: The firmware for this device is mostly complete.
  - Monitor FPGA: The firmware has not yet been started, as it clearly has a lower priority.
  - VME FPGA: The firmware has been started.
  - VME CPLD: The coding has been completed
- The first assembled 9U ROD module itself arrived at RAL last week, and visually looks fine. A small number of minor bugs have been sorted out, and the JTAG boundary scanning has just started, so far successfully.
- The order for the second 9U ROD module to be assembled will be placed as soon as the first module is pronounced to be working.
- Tony noted that there would be internal Final Design Reviews of the TCM and VMM coming soon, probably in October 2004, for which reviewers would be sought. Adam has been making the necessary design changes to the schematics of these two modules, but this work is not yet complete.
- Adam has circulated a document summarising the options for choice of CANbus microcontroller in the trigger modules, with the aim of reaching an early consensus for using a common device.
- A provisional final order for TTC modules has been placed with Philippe Farthouat: to instrument a maximum of six Test Rigs during ATLAS operation, another four TTCex modules and one more TTCvi module will be needed. A revised estimate of the final number of TTCrx chips needed will be made, and double-checked with the provisional number originally requested from Philippe a long time ago.
- Bruce asked how many Wiener 9U crates had been ordered for Test Rigs. One VME64x crate and two custom-Backplane Processor crates were ordered. We will need to re-use some of the prototype Processor crates.

5. Stockholm

- Attila reported that the JEM achieved reliable 16-bit G-link locking and data transfers when operated from non-TTC clocks, after firmware changes to create fully-asynchronous FIFO data buffering. With the four unused bits masked off in the ROD, error-free runs of several hours were achieved. However, operation of the 20-bit G-links at RAL still exhibited instabilities, and some clock phase/timing changes will be needed.
- Sam has successfully tried out the proposed repair procedure for damaged connector pins on the small prototype stub Backplane, using the purpose-built tool which he purchased. He would now like to try out the procedure on an full Processor Backplane.
- The design and implementation of the new power bus-bar system appears to be very sound.
- The cable/connector strain relief system for the Processor Backplane, which uses stainless steel forks, also seems to work well, and it would be good to try this out on an actual partially cabled Processor Backplane as soon as possible – hopefully when Sam visits RAL in October for the Processor Backplane Final Design Review.
- Sam is expecting very soon to receive in Stockholm the two Wiener 9U Processor crates which have just been shipped from CERN after passing their acceptance tests.

Next Phone Conference – Thursday 9th September 2004 at 10:00 (UK), 11:00 (Germany, Sweden)

Tony Gillman