Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 27th February 2004

Birmingham:	**Gilles Mahout, Richard Staley, Dimitrios Typaldos, Pete Watkins**
Heidelberg:	**Ralf Achenbach, Florian Föhlisch, Paul Hanke, Kambiz Mahboubi, Frederik Rühr, Klaus Schmitt**
Mainz:	**Cano Ay, Stefan Rieke, Uli Schaefer**
RAL:	**Bruce Barnett, Ian Brawn, Norman Gee, Tony Gillman, Adrian Mirea, Weiming Qian**

1. Birmingham

- There is a significant problem of loss of CPM-ROD G-link lock during long data runs, which is believed to be caused by excessive jitter on the TTC clocks when derived from the TTCdec cards. Studies show that the current design of TTCdec cards exhibit a deterministic jitter component in addition to the expected random jitter component. The magnitude of this extra component varies between different TTCdec cards, and has been observed to be as high as 500 psec. Its incidence scales non-linearly with the L1A rate (up to the maximum possible 130 kHz), which produces significant TTC traffic. Additional PLLs are unable to reduce the effect, and in fact can worsen it. Furthermore, there is also some evidence that it reduces the already narrow backplane timing margins in the current CPMs, so a solution must be found.

  One suggestion is to measure the jitter on all assembled TTCdecs (~20), and to use the lowest-jitter cards on the CPMs. However, there may not be sufficient (or any) cards with low enough jitter to fix the problem for the Slice Tests and Test Beam running, since the CMMs and 6U RODs (is the TTC clock used for driving the S-links?) may also need low-jitter cards. If not, the current TTCdec card (Mk 2) must be redesigned. Note that Weiming's new TTCdec design (Mk 3) appears fine, and this effect is absent on all four of the cards measured so far. The differences are: i) in the Mk 3 design, all three "analogue" power pins on the TTCrx chip are fed from a filtered supply, whereas in the Mk 2 cards one of these pins is incorrectly fed from the "digital" supply, ii) the Mk 2 cards have been assembled with an incorrect component value in the recommended high-pass filter network before the TTCrx chip. It would be nice to know how the deterministic jitter component is getting into the clocks so that a TTCdec card redesign can prevent it.

2. Heidelberg

Paul was welcomed back, and he reported on the status of hardware at KIP.

- The results of the LAr/TileCal receiver tests have been written up by Frederik, and will be circulated to the level-1 community next Monday. They describe the distorting effects of the receiver on saturated pulses, making BCID impossible. The solution is to change the time constant of the internal low-pass filter from 15 nsec to 5 nsec, and when this and other changes have been made next week the BCID performance will be re-evaluated. The LAr/TileCal receiver will have a PRR at CERN on Monday 8th March.
- The first four PPM PCBs have been manufactured, and one has already been partly assembled at KIP (ReM FPGA, 25% of the MCM connectors, etc). The surface finish of the boards looks very good by eye. The first module will be powered up on the bench today.
- As the assembly company are not satisfied with the quality of the gold pad surface finish on the new batches of MCM substrates, it has been decided to send two test samples from each of the two substrate manufacturers (Wurth and Dyconex) to an independent analysis company for further assessment and tests. Results will be known by 8th March, when there will also be a meeting with Wurth to discuss the reasons for the disturbingly low yield (30%) of "good" substrates.
- On 24th February a meeting had been held with representatives from Wiener to discuss the VME64x crate requirements for the PPr. The conclusion was that the number of power pins on J1 and J2 in the "standard" VME64x backplane is not sufficient to provide comfortable headroom for

the large +5V current needed by each PPM, so the VME64xP (VIPA) backplane variant, providing extra power pins on J0, would be ordered to ensure an adequate safety margin. Sufficient supplies of the VIPA backplanes are available ex stock, so a quotation has been obtained from Wiener for eight crates (with power supplies) plus two test crates/power supplies, with a number of spare components (including two spare backplanes. If in the long-term (years) there were a need for replacement backplanes (due to damage, etc) and the VIPA variants were no longer available, it would be possible to modify a "standard" VME64x backplane by adding a customised J0 backplane segment with the necessary +5V pins and a bus-bar.

The order is expected to be placed with Wiener before 31st March, for delivery in two batches starting June 2004.

- It was confirmed that the ReM FPGA firmware would conform to the latest data format specifications.
- The PPMs to be used for the Slice Tests and Beam Tests will be populated with MCMs loaded with the original PPr ASIC dies, i.e. with the known parity bit error. (This bug has been corrected in the re-designed ASICs, but these will only be assembled into the production MCMs.)

3. Mainz

- The first JEM1 module is expected back from assembly next week, and everything is ready at Mainz to start testing it.
- The first Input daughter-card has been thoroughly tested, with an excellent measurement on all LVDS links of BER < 10**-14. Three more Input daughter-cards will now be assembled for the first JEM1.
- The design and layout of the daughter-cards carrying the DAQ and RoI G-links and optical transmitters is almost complete, and two cards will be manufactured and assembled, starting next week.

4. RAL

- Firmware incorporating the new VME mapping for the CP and Energy versions of the CMM has been supplied to Sam in Stockholm.
- The engineer to replace Panagiotis, who leaves RAL at the end of February, is Ed Freeman. He will start to design the CPLD code for the new ROD VME interface.
- The major effort on firmware design for the new ROD will be starting next week.
- A commercial system for firmware version management (Synchronicity) is being evaluated.
- Manufacture of the PCBs for the new CPM design (CPM1.5) will be completed next week. Assembly will follow immediately, once the important temperature profiling has been carried out at the company using one of the current (non-working) CPMs – CPM#3.

Next Phone Conference – 26th March 2004 at 10:00 (UK), 11:00 (Germany, Sweden)

Tony Gillman